Growth, Thermodynamics, and Electrical Properties of Silicon Nanowires†

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1. Introduction

Research on silicon nanowires has developed rapidly in recent years. This can best be inferred from the sharply increasing number of publications in this field. In 2008, more than 700 articles on silicon nanowires were published, which is twice the number published in 2005. Because of this strong increase in research activities and output, the vast majority of publications on silicon nanowires are found to be younger than ten years. At first glance, one could therefore be tempted to assume that Si nanowire research is a very young research field. This, however, is not the case. Si nanowire research had a rather long incubation period before it became a fashionable subject, driven by potential applications in nanoelectronics and sensors.

The review, which to our knowledge is the first on silicon wires, dates back to the late 1950s.[1] Therein, Treuting and Arnold reported the successful synthesis of ⟨111⟩ oriented Si whiskers. The term whisker was at that time the commonly used expression when reference was made to filamentary crystals. Nowadays, the term whisker has almost disappeared. Instead, the terms "wire" and "nanowire" have found widespread use. In this article, we will adopt this newer

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Ulrich Gösele was Director of the Experimental Department II at the Max Planck Institute of Microsctructure Physics, Halle, Germany, Honorary Professor of Experimental Physics at Martin Luther University Halle-Wittenberg, Germany, as well as Adjunct Professor of Materials Science at Duke University's School of Engineering, Durham, North Carolina. While staying with the Max Planck Institute of Metal Physics, Stuttgart, Germany, he received his Ph.D. from the University of Stuttgart in 1975. Afterward, he worked as a researcher for Siemens (Munich, Germany), IBM (Yorktown Heights, New York), NTT (Japan), and a nuclear research center in South Africa. In 1985, he became Full Professor of Materials Science and, later on, J. B. Duke Professor of Materials at Duke University, Durham, NC. Since 1993, he was a Scientific Member of the Max Planck Society and Director at its Max Planck Institute of Microstructure Physics in Halle. Ulrich Gösele was a Fellow of the American Physical Society and Great Britain's Institute of Physics. He was a member of the German National Academy of Sciences and was on the board of the Materials Research Society in the USA. He passed away in November 2009.

terminology. Rodlike crystals with a diameter of less than 100 nm will be referred to as nanowires. In places where rodlike crystals of larger diameters are considered, the term wire will be used. The term wire will also be used in a generalized sense, i.e. when reference is to be made to both wires and nanowires.

Regarding silicon wire growth, it is remarkable to see how much was already known in the 1960s. The best example of this is the vapor−liquid−solid mechanism of Si wire growth proposed by Wagner and Ellis in their seminal article published in March 1964.[2] Till today, the vapor−liquid−solid (VLS) growth mechanism was the most prominent method for silicon wire synthesis. The VLS mechanism really represents the core of silicon wire research, though it does not only work for silicon but also for a much broader range of wire materials. The VLS mechanism can best be explained on the basis of Au catalyzed Si wire growth on silicon substrates by means of chemical vapor deposition (CVD) using a gaseous silicon precursor such as silane.

The Au−Si binary phase diagram possesses a characteristic peculiarity, namely that the melting point of the Au−Si alloy strongly depends on composition. A mixture of 19 atom % Si and 81 atom % Au already melts at 363 °C, which is about 700 K lower than the melting point of pure Au and more than 1000 K lower than the melting point of pure Si. Thus, heating Au in the presence of a sufficient amount of Si, considering e.g. a Au film on a Si substrate, to temperatures above 363 °C will result in the formation of liquid Au−Si alloy droplets as schematically depicted in Figure 1a. Exposing these Au−Si alloy droplets to a gaseous silicon precursor such as silane, SiH_4, will cause precursor molecules to preferentially crack at the surface of these droplets, thereby supplying additional Si to the droplet. At equilibrium the phase diagram allows only for a limited amount of Si

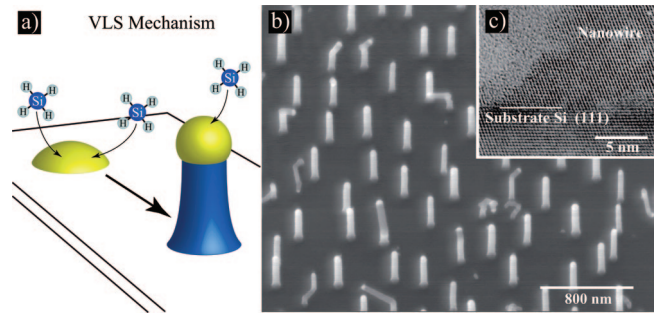


Figure 1. (a) Schematics of the vapor−liquid−solid growth mechanism. (b) Scanning electron micrograph of epitaxially grown Si nanowires on Si ⟨111⟩. Transmission electron micrograph of the interface region between Si nanowire and substrate. Note the epitaxy and the curved shape of the nanowire flank. Parts b and c are reprinted from ref 3 with permission from Zeitschrift für Metallkunde, Carl Hanser Verlag, München.

dissolved in the Au−Si droplets. The additional supply of Si from the gas phase therefore forces the droplets to find a way of how to dispose of the excess Si. This is accomplished by crystallizing solid Si at the droplet−wire interface. A continuous supply of Si consequently leads to the growth of wires with a Au−Si droplet at their tip, as schematically indicated in Figure 1a.

The name vapor−liquid−solid (VLS) mechanism reflects the pathway of Si, which coming from the vapor phase diffuses through the liquid droplet and ends up as a solid Si wire. Related is the so-called vapor−solid−solid (VSS) mechanism, which describes cases where a solid catalyst particle instead of a liquid droplet is involved. An example of Au-catalyzed Si nanowires grown homoepitaxially on a ⟨111⟩ substrate via the VLS-mechanism is shown in Figure 1b. These nanowires were grown at about 450 °C using silane as precursor.[3] The transmission electron micrograph in Figure 1c proves the epitaxial relation between nanowire and substrate. What should also be noted in Figure 1c is the curved shape of the nanowire flank; an aspect that will be discussed in detail later on in section 7. The most remarkable feature of the VLS growth mechanism, however, is its universality. VLS growth works well for a multitude of catalyst and wire materials and, regarding Si wire growth, over a size range of at least 5 orders of magnitude; from wire diameters of just a few nanometers up to several hundred micrometers.

The VLS mechanism has numerous direct and indirect implications for Si wire growth. Consequently, a large part of this review, which is an extended version of a previous article,[4] focuses on the limitations and implications of the VLS mechanism. This concerns experimental issues such as the choice of growth method (section 2) and catalyst material (section 3), the crystallography of the wires (section 4), and the synthesis of heterostructures (section 5), as well as theoretical issues such as the depression of the eutectic temperature (section 6), the expansion of the wire base (section 7), the surface tension criterion (section 8), and the Gibbs−Thomson effect (section 9). The last part of this article deals with the electrical properties of silicon nanowires: from nanowire doping (section 10) and the question of dopant ionization (section 11) to the influence of surface states on the effective charge carrier density (section 12).

2. Silicon Nanowire Synthesis Techniques

Different techniques for silicon nanowire synthesis were developed in the past, with chemical vapor deposition (CVD) being just one of them. Which growth method is suited best depends on the application in mind as well as on the intrinsic capabilities and limitations of the technique in question. In this section, we therefore want to take a closer look at the different growth techniques and their particular advantages and disadvantages.

The different growth techniques mainly differ in the way silicon is supplied. There are two possibilities, either wire growth is fed directly by elemental silicon or silicon is provided as a silicon compound. It is clear that in the latter case a chemical reaction has to take place at the catalyst particle to initiate wire growth. Silicon itself is very sensitive to oxidation. Depending on whether oxygen-rich or nominally oxygen-free conditions are applied, growth results differ strongly. It therefore turns out to be convenient to distinguish between the use of oxygen-rich and oxygen-free Si precursors. In the following, the term chemical vapor deposition will only be applied to the use of oxygen-free precursors. Oxygen-rich precursors, such as, for example, SiO, shall be excluded by definition and dealt with separately. Of course, one could argue that using SiO as precursor also represents some sort of chemical vapor deposition; nevertheless, for practical reasons, we will make this distinction here.

2.1. High Temperature Chemical Vapor Deposition

In chemical vapor deposition (CVD), as defined above, the necessary silicon for wire growth is provided by an oxygen-free precursor. The most frequently used precursors are silane, SiH_4, disilane, Si_2H_6, dichlorosilane (silicon dichloride), SiH_2 Cl_2, and tetrachlorosilane (silicon tetrachloride), $SiCl_4$. Replacing hydrogen atoms by chlorine mainly comes with two effects. The first, almost trivial, effect is that the use of a chlorinated silane precursor in the presence of hydrogen will lead to the creation of hydrochloric acid during nanowire processing; and hydrochloric acid usually causes some desirable or undesirable etching of the substrate, the nanowires, and the equipment. The second is related to the fact that chlorinated silanes are, generally speaking, chemically more stable than their nonchlorinated counterparts.[5] Consequently, higher temperatures need to be applied to thermally crack the precursor. For tetrachlorosilane, $SiCl_4$, growth temperatures typically range from about 800 °C[6−9] to well beyond 1000 °C,[10,11] compared to temperatures of about 400−600 °C, typical for Si wires grown in the presence of silane.[3,12,13] In view of this difference in process temperature, which, for example, affects the choice of the catalyst material, the discussion on chemical vapor deposition is split into a high temperature and a low temperature part; with high temperature being defined as covering temperatures higher than about 700 °C.

High temperature CVD Si wire growth experiments are often performed in tubular hot wall reactors.[7−9,11] As schematically depicted in Figure 2a, a gas flow—typically hydrogen or a hydrogen/inert gas mixture—is directed through an externally heated quartz tube held at about atmospheric pressure. Prior to entering the reactor, a part of the gas is led through a bubbler filled with $SiCl_4$ ($SiCl_4$ is liquid at room temperature and atmospheric pressure), thereby supplying $SiCl_4$ to the reactor. If a Si sample, onto which some amount of the catalyst metal has been deposited beforehand, is placed in the hot zone of the reactor, silicon wires will commence growing. An excellent example of what can be achieved this way can be seen in Figure 2b, which shows a scanning electron microscope (SEM) image reprinted from the work of Kayes et al.[7] The almost optimal arrangement of the homoepitaxially grown, Cu-catalyzed Si wires, based on an appropriate arrangement of the catalyst by lithography, is striking. There are reports that homoepitaxial growth of Si wires on Si substrates is facilitated by the use of $SiCl_4$ if used in combination with H_2,[8] as the developing HCl gas can etch away an unwanted oxide coverage of the substrate.

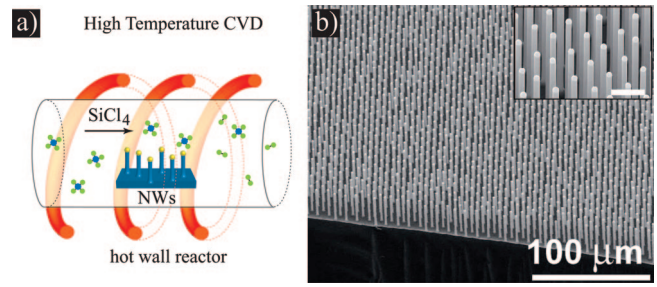


Figure 2. (a) Schematic setup of high temperature CVD. (b) Tilted scanning electron micrograph of a Cu-catalyzed Si wire array. The scale bar in the inset is 10 μm. Part b was reprinted with permission from ref 7. Copyright 2007 American Institute of Physics.

Historically, high temperature CVD via $SiCl_4$ was preceded by experiments using a closed reaction vessel instead of a flow reactor. Wagner et al.[14] and Greiner et al.,[15] for instance, obtained their early results by using evacuated and sealed quartz ampules into which iodine was placed together with silicon and the catalyst material. Upon heating, iodine reacts with silicon to form gaseous silicon iodide products, which then serve as a locally produced CVD precursor. Silicon wire growth takes place at the colder parts of the quartz ampule. This version of high temperature CVD, mentioned here for the sake of completeness, is attractive for its technical simplicity and low cost—assuming an apparatus for sealing evacuated quartz ampules is at hand.

Like most thermally activated processes, also Si wire growth using Au as catalyst and $SiCl_4$ as precursor shows an Arrhenius-type exponential dependence on process temperature ($\propto \exp(-E_a/kT)$), with E_a being the activation energy and kT having its usual meaning. The data of Wagner et al.[16] indicate an activation energy E_a of about 32 ± 1 kcal/mol (1.38 ± 0.06 eV), which is slightly smaller than the activation energy of 37 kcal/mol obtained by Theuerer[17] for Si layer deposition using $SiCl_4$. Due to the exponential temperature dependence of the Si wire growth velocity and the high temperatures applied, growth velocities can be quite substantial. Often wire growth velocities on the order of μm/min[7,10,18] or even μm/s[11] are observed. Although this is not of major concern considering the growth of Si wires with micrometer lengths, such high growth velocities represent a restriction for the controllability if synthesis is aimed at Si nanowires of submicrometer lengths.

Another effect of the elevated temperatures is related to the diffusion of the catalyst metal. It is generally known that metal clusters, islands, or droplets on a surface tend to agglomerate; a phenomenon usually referred to as Ostwald ripening.[19−23] Considering the growth of Si wires via the VLS mechanism, Ostwald ripening causes the larger catalyst droplets to grow (ripen) at the expense of the smaller ones.

The speed at which this ripening proceeds depends on the rate at which the different catalyst droplets can exchange material with each other. That means, for wire growth on a substrate, that ripening mainly depends on surface diffusion, which can be expected to be faster at higher temperatures. As a consequence of the Ostwald ripening of the catalyst droplets, it becomes exceedingly more difficult to grow nanowires with well-defined diameters at elevated temperatures—simply because the droplet size does not stay constant during processing. This has been reported, for example, by Kayes et al.,[7] who deposited a regular array of Au-dots on a bare Si substrate. Upon heating, the droplets agglomerated, thereby destroying the regularity of the arrangement. To prevent/minimize droplet agglomeration, Kayes et al.[7] had to deposit an additional SiO_2 layer, serving as a diffusion barrier for the catalyst material. Not only does surface diffusion, however, affect the initial catalyst size, but also growth itself might be affected, as catalyst material can diffuse to neighboring wires.[24,25] In view of the problems related to catalyst diffusion, high temperature CVD seems to be more suited for the growth of microscopic Si wires rather than nanowires; though high temperature CVD growth of nanowires with diameters of about 40 nm has nevertheless been demonstrated.[8]

The main advantage of high temperature CVD consists in the much broader choice of possible VLS catalyst materials. Au and Cu[7,16] yield excellent results at temperatures above 850 °C (see Figure 2b). At even higher temperatures, also Pt and Ni seem to be a good choice.[16] A more thorough discussion on the choice of catalyst materials will be given in section 3. Independent of the catalyst material used, the main crystallographic growth direction of these nanowires appears to be the ⟨111⟩ direction,[8,16,17] probably because of the large diameter of the wires.[26,27] The corresponding wires are typically single crystalline and free of crystallographic defects. Wagner et al.,[16] however, point out that also ⟨112⟩ orientated wires, showing a twin defect parallel to the wire axis can be found.

A doping of the growing wire directly from the gas phase is possible, even at high temperatures. Givargizov reports the use of $AsCl_3$[10,28] and PCl_3[10] as vapor phase dopants. Interestingly, the introduction of the dopant precursor does influence the wire morphology. Givargizov points out that the periodic instability of the wires (a periodic variation of the wire diameter observed at high temperatures and pressures) disappears once $AsCl_3$ is added to the gas mixture,[28] presumably because $AsCl_3$ changed the surface tension configuration of the wire and/or the catalyst droplet.

2.2. Low Temperature Chemical Vapor Deposition

Low temperature chemical vapor deposition (CVD) shall comprise the growth temperatures lower than 700 °C. The typical precursors for low temperature CVD are silane (SiH_4) and, though less frequently, disilane (Si_2H_6). In contrast to tetrachlorosilane, silane already decomposes at about 350 °C so that the temperature range from the Au−Si eutectic at 363−700 °C is fully covered. Another noteworthy difference to $SiCl_4$ is that both silane and disilane are self-igniting gases that are potentially explosive if brought into contact with air. Thus, working with silane or disilane requires great care to prevent issues with machinery or personnel.

The most frequently used catalyst material for VLS Si nanowire growth is Au. Using Au and silane, homoepitaxial

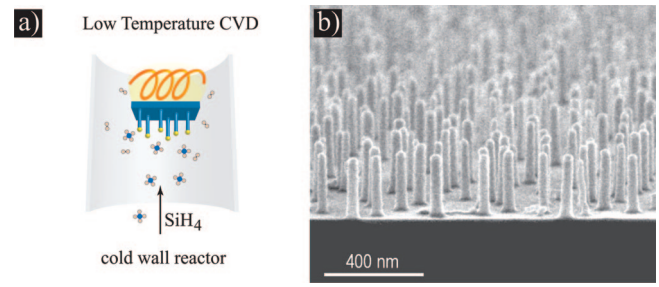


Figure 3. (a) Schematic of a low temperature chemical vapor deposition reactor. (b) Al-catalyzed Si nanowires on Si⟨111⟩ grown at about 430 °C. Part b is reprinted from ref 95. Copyright 2006 Macmillan Publishers LTD: Nature Nanotechnology.

growth of Si wires or nanowires can be achieved without much difficulty (see Figure 1b), provided that the native oxide, naturally covering silicon substrates, is removed prior to the Au deposition. Wire diameters from a few nanometers up to several micrometers can be realized. The dominant orientation of wires with diameters larger than about 50 nm orientation is ⟨111⟩.[26,27] More details on the crystallography are given in section 4.

Often dedicated, low pressure, cold wall reactors are used, as schematically shown in Figure 3a. For the use of Au as catalyst, high-vacuum equipment (base pressure around 10^{-6} mbar) is sufficient for growing nanowires. This is, however, not the case when more sensitive catalyst materials are used. Aluminum, for instance, is very sensitive to oxidation, so that the use of an ultrahigh-vacuum reactor with a base pressure lower than about 10^{-9} mbar is recommended. Yet, if oxidation of Al is prevented, excellent results can be achieved with Al as catalyst; see, for example, Figure 3b.

Typical silane partial pressures range from 0.1 mbar to 1 mbar,[12,27,29] which results in growth velocities on the order of nanometers per second. Concerning the pressure dependence, the data published by Lew et al.[12] indicate that the growth velocity increases approximately linearly with silane partial pressure. Nanowire growth velocities related to the use of silane as precursor show an exponential dependence on inverse temperature ($\propto \exp(-E_a/kT)$). From observations at growth temperatures of 450−600 °C, Schmid et al.[29] deduced an activation energy, E_a, of 19 ± 1.5 kcal/mol (0.82 ± 0.07 eV). Lew et al.[12] investigated nanowire growth at a similar temperature range and reported an activation energy of 22 kcal/mol. However, their data seem to indicate a somewhat smaller value, closer to the 19 kcal/mol of Schmid et al.[29] From the data of Bootsma and Gassen,[30] who studied Si nanowires growth at temperatures of 600−800 °C, an activation energy of 11.1 ± 0.4 kcal/mol (0.48 ± 0.02 eV) can be deduced.

Combining the pressure and temperature dependencies,[12,29] one can obtain the following estimate for the temperature and pressure dependence of the growth velocity of Au-catalyzed nanowires:

$$v \approx 1.7 \times 10^6 \frac{\text{nm}}{\text{s mbar}}\, p \exp\left(\frac{-9500\ \text{K}}{T}\right) \qquad (1)$$

with p being the silane partial pressure in millibar; see Figure 4. This formula serves only as a crude estimate for practical use. The accuracy is presumably not much better than a factor of 2. One should furthermore keep in mind that the growth velocity also depends on the nanowire diameter (see section 9) and other parameters.

Si nanowires obtained by using Au and silane are usually only slightly tapered, which indicates that radial growth is

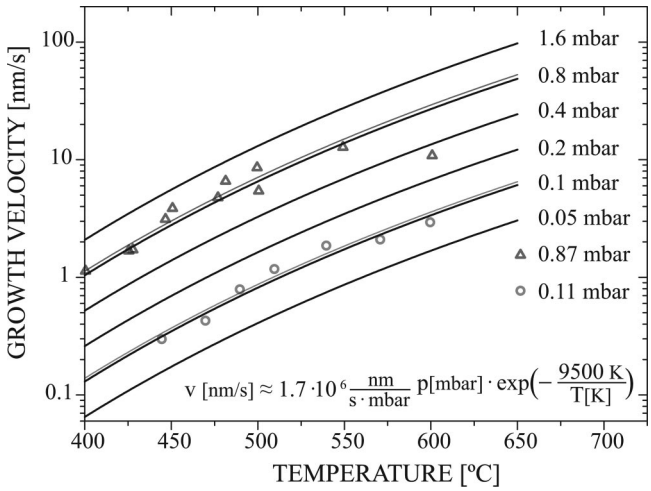


Figure 4. Approximate Si nanowire growth velocity (using Au as a catalyst) as a function of pressure and temperature using data from Lew et al.[12] (triangles) and Schmid et al.[29] (circles).

slow compared to axial growth. According to the data by Schmid et al.,[29] radial growth rates are about 2 orders of magnitude smaller than axial growth rates. The activation energy for radial growth is found to be larger than that for axial growth. Schmid et al.[29] determined a value of 29 ± 3 kcal/mol (1.26 eV). This value is still slightly smaller than the activation energy of 35.4 kcal/mol derived from silicon thin film deposition experiments using silane.[31,32] The fact that the activation energy of radial growth is still smaller than the nominal activation energy for Si thin film deposition could possibly be explained by the catalytic effect of a Au contamination of the nanowire surface.[24]

Another attractive precursor for low temperature CVD is disilane, Si_2H_6. Disilane is more reactive than monosilane, SiH_4. Silicon thin film deposition experiments gave an activation energy of 28.4 kcal/mol (1.23 eV) compared to 35.4 kcal/mol (1.53 eV) for silane.[31,32] The higher reactivity of disilane compared to silane represents its main advantage, as it allows for Si wire growth at much lower pressures compared to that for silane. The lower pressures are particularly important for the in situ observation of Si nanowire growth, for example, in a transmission electron microscope (TEM).[24,33−35] Kodambaka et al.[36] investigated the diameter, temperature, and pressure dependence of the nanowire growth velocity. They grew Au-catalyzed nanowire at disilane partial pressures as low as 2×10^{-8} Torr, corresponding to a growth velocity of about 1 nm/min. From the temperature dependence, they deduced an activation energy of 12.2 ± 0.5 kcal/mol (0.53 ± 0.02 eV).[36]

In summary, one should keep in mind that the activation energies for Au-catalyzed Si nanowire growth are about half as large as those for Si thin film growth: 19 kcal/mol vs 35 kcal/mol for silane and 12 kcal/mol vs 28 kcal/mol for disilane. This reduction by about a factor of 2 is what makes the Au droplet a catalyst droplet.

Doping of silicon nanowires directly from the vapor phase is also possible for low temperature CVD. Often phosphine, PH_3, or diborane, B_2H_6, is used to that end. Due to the crucial importance of a proper doping for the electrical properties, doping will be discussed in detail in section 10.

One subclass of low temperature CVD that requires mentioning here is plasma enhanced CVD (PECVD).[37−40] By means of a plasma in the nanowire growth reactor, the silicon precursor, silane in most cases, is partially precracked.

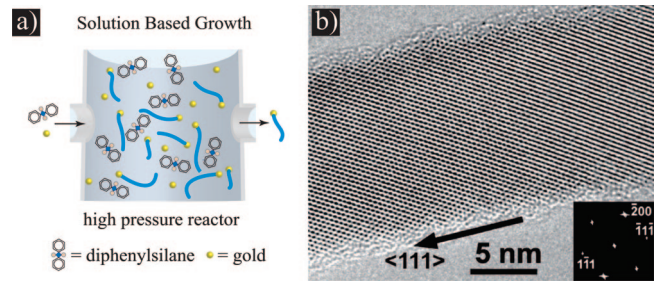


Figure 5. (a) Schematic setup for solution-based growth of Si nanowires. (b) Transmission electron micrograph of a Si nanowire grown from solution. Part b is reprinted with permission from Tuan et al.[54] Copyright 2008 American Chemical Society.

Such a precracking facilitates and enhances the supply of Si to the catalyst droplet. PECVD turns out to be a successful method for the low temperature synthesis of Ga- or In-catalyzed Si nanowires.[37−40]

The advantages of low temperature CVD are that nanowires with a large variety of diameters and lengths can be grown epitaxially on Si substrates. With the lengths of the wires being essentially proportional to the process time, they can be easily adjusted. Nanowire growth at predefined positions on the substrate is possible.[29,41] Furthermore, the electrical properties of the nanowires can be tuned directly by doping from the gas phase,[29,42,43] allowing also for modulated doping profiles.[44] One of the major problems of epitaxially grown Si nanowires is that they exhibit a certain variation of the growth direction, especially for diameters smaller than about 50 nm.[27] A related, ubiquitous problem is that a certain percentage of the nanowires tends to change their growth direction during growth; as a result, they show a kink (see Figure 1b).[29,45,46] This kinking problem, however, can be circumvented by growing the nanowires inside a template such as anodic aluminum oxide (AAO).[47−49] The template forces the nanowire to grow straight along the pore direction. This approach also leads to epitaxial ⟨100⟩ oriented nanowires, an orientation usually not favored by free-standing nanowires.[49]

2.3. Supercritical-Fluid-Based and Solution-Based Growth Techniques

Approaches similar to chemical vapor deposition are the so-called supercritical-fluid-based and solution-based growth techniques, developed in the group of Korgel.[50] In their original design, diphenylsilane, $SiH_2(C_6H_5)_2$, was used as Si precursor, which was mixed with hexane and sterically stabilized gold nanoparticles in a high pressure reactor. High pressures of 200−270 bar and a temperature of 500 °C were applied to the reaction vessel. Under these conditions, hexane becomes supercritical, which is why this method is referred to as being supercritical-fluid-based.

The synthesis is often performed in a way that a flow reactor[51,52] such as that sketched in Figure 5a is used instead of a closed reaction vessel. In this case, gold colloid particles together with a well-defined amount of the Si precursor, e.g. diphenylsilane, are fed into the solution as dispersions and transferred into the heated and pressurized reactor, where the nanowire synthesis takes place. The fact that nanowire synthesis can be performed in a continuous process instead of a batch process is one of the inherent decisive advantages of this method. Furthermore, the variability with respect to the choice of the precursor offers an additional degree of

freedom for optimization. Lee et al.,[53] for example, reported that the results using monophenylsilane, SiC_6H_8, and diphenylsilane as precursor differ in that the use of monophenylsilane leads to a higher product yield and additionally to a smaller amount of carbonaceous byproduct as compared to using diphenylsilane.

Using the method described above, Si nanowire growth is assumed to proceed via the supercritical-fluid−liquid−solid (SFLS) growth mechanism, the equivalent to the vapor−liquid−solid (VLS) growth mode explained before. As in VLS nanowire growth, nanowire diameters can be adjusted by the size of the metal nanoparticles, serving as catalysts. The fabrication of single crystalline nanowires with diameters as low as 5 nm and lengths of several micrometers has been demonstrated.[52] A high resolution transmission electron micrograph of a Au-catalyzed silicon nanowire grown via the SFLS mechanism using monophenylsilane as precursor[54] is reprinted in Figure 5b. Please note the perfect crystallinity of the nanowire.

Having the vapor−solid−solid (VSS) mechanism in mind, one would expect that Si nanowire growth in supercritical fluid can also be mediated by a solid catalyst particle; and, indeed, this is the case. Growth of Cu-, Ni-, and Co-catalyzed Si nanowires performed at temperatures well below the melting point of the corresponding metal-Si alloy has been demonstrated.[55,56]

Another very attractive approach for the high yield production of nanowires is solution-based nanowire growth, a good example of which has been published very recently. Heitsch et al.[57] demonstrated the Au- and Bi-catalyzed growth of silicon nanowires in solution at atmospheric pressure. Trisilane, Si_3H_8, which is even more reactive than disilane, is used as silicon precursor. The growth reaction takes place in a vessel filled with a long-chain, low-vapor-pressure hydrocarbon. Nanowire synthesis temperatures higher than the eutectic temperatures of Au−Si or Bi−Si were applied, so that, analogously to the VLS mechanism, a solution-liquid−solid mechanism can be assumed.[57] Using the above-described method, Heitsch et al. demonstrated the synthesis of micrometer long, crystalline nanowires with diameters of about 25 nm.[57]

The main advantages of this method are that thin nanowires of good crystalline quality can be synthesized in large amounts using comparably simple equipment. Compared to other nanowire synthesis methods, the yield is excellent. The only disadvantage is that a controlled, in-place, epitaxial growth can hardly be realized.

2.4. Molecular Beam Epitaxy

A further Si nanowire growth technique is molecular beam epitaxy (MBE).[58−62] Here, elemental Si, instead of a chemical Si compound, serves as the source for Si nanowire growth. Si nanowire growth is achieved by evaporating Si onto a catalyst covered substrate, typically Si⟨111⟩, as illustrated in Figure 6a. To prevent oxidation or contamination of the substrate or the nanowires, an ultrahigh vacuum (UHV) system with a base pressure in the 10^{-10} mbar range is typically used for MBE. To maintain such low pressures even during nanowire processing, parts of the system are often additionally cooled with liquid nitrogen.

Preceding Si evaporation, Au is deposited onto the substrate. Annealing the substrate at temperatures above the Au−Si eutectic temperature causes the Au film to break up. Au mixes with Si from the substrate, and Au−Si alloy

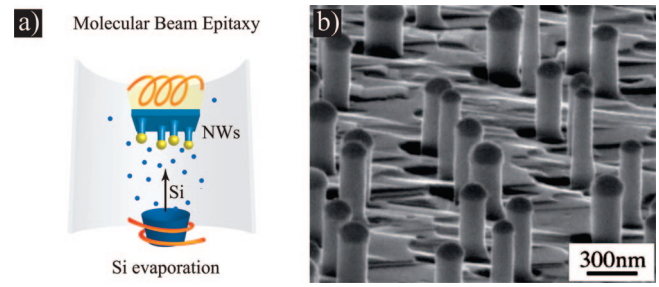


Figure 6. (a) Schematics of MBE Si nanowire growth. (b) Scanning electron micrograph of Au-catalyzed Si nanowires on Si⟨111⟩. Part b is reprinted from ref 59 with permission from Elsevier.

droplets form, which then act as catalysts for the subsequent VLS Si nanowire growth. Since MBE does use elemental Si instead of a chemical compound as Si source, the role of the Au catalyst merely consists of facilitating Si crystallization. From a chemical point of view, one could argue that the catalyst droplets are not real catalysts anymore, as there is no chemical reaction involved. However, the fact that the Si nanowires grow faster than the substrate by about a factor of 2—a fact that is not obvious in the first place—indicates that the catalyst droplets do have an effect on Si crystallization.

Typically, Si nanowires are grown at substrate temperatures of 500−700 °C.[58,60,63,64] The necessary Si evaporated onto the substrate diffuses on the substrate surface until it either crystallizes directly or finds a Au catalyst droplet. MBE growth of Si nanowires therefore strongly relies on Si surface diffusion, which is the main reason why growth temperatures higher than 500 °C are used. Yet, at these temperatures, it is difficult to realize small Au−Si droplet sizes (due to Ostwald ripening), and the diameters of the nanowires therefore usually exceed 40 nm. Another potential cause for the fact that only nanowires with diameters larger than about 40 nm can be obtained[58,62] is the Gibbs−Thomson effect, as discussed in section 9.

The fact that Si nanowire growth depends on Si surface diffusion has direct implications for the nanowire growth velocity. As surface diffusion is a rather slow process, one can expect the nanowire growth velocities to be comparably small; typically growth velocities of 1−10 nm/min are realized.[60,63] The second implication concerns the diameter dependence of the growth velocity. If the areal density of Si adatoms diffusing toward the catalyst droplet is taken to be constant, then the amount of Si per unit time reaching the droplet is proportional to the circumference of the nanowire. Moreover, at a given Si supply rate, the growth velocity has to be inversely proportional to the nanowire cross-sectional area. Combining both, it becomes immediately clear the growth velocity should be inversely proportional to the nanowire diameter. And this also has been observed.[58]

In general, Si nanowires grown by MBE are single crystalline and ⟨111⟩ oriented. They can be grown homoepitaxially on Si without much problem. Nanowire growth at predefined positions on the substrate is possible.[61] The advantages of MBE are clearly that the fluxes can be accurately controlled. A precise control of the incoming particle fluxes is particularly important for a doping of the nanowires. When the MBE system is equipped with evaporation sources for Si dopants such as B or Sb, Si nanowires with well controlled doping profiles can be realized.[65] If additional evaporation sources, for example, for Ge, exist, also axial nanowire heterostructures can be achieved by simply switching sources.[59]

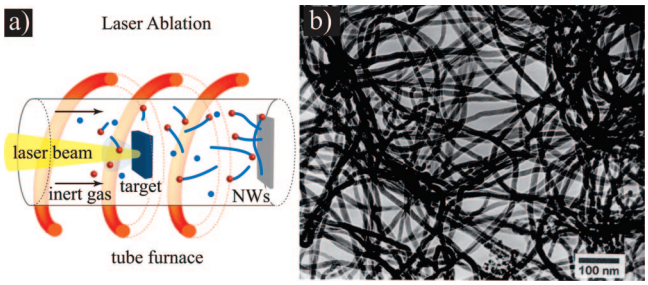


Figure 7. (a) Schematic of a laser ablation setup. (b) Transmission electron micrograph of Si nanowires grown by laser ablation. Part b is reprinted with permission from ref 235. Copyright 1999 American Institute of Physics.

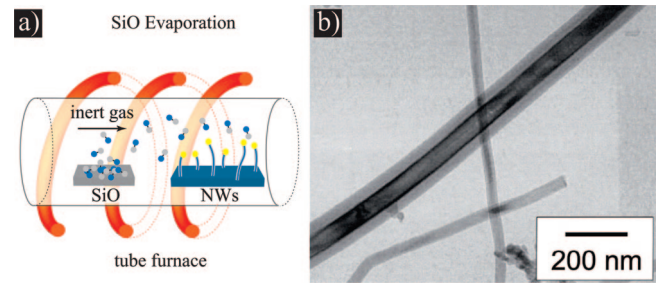


Figure 8. (a) Schematic of a setup of nanowire growth via SiO evaporation. (b) Transmission electron micrograph of a thick silicon nanowire with its crystalline silicon core and the thick amorphous oxide shell. Part b is reprinted from ref 83. Reproduced with permission of The Electrochemical Society.

The main disadvantages of Si nanowire synthesis via MBE are the considerable Si film growth on the substrate and the limited flexibility concerning nanowire diameters and aspect ratios; see Figure 6b. The rather limited aspect ratios are due to the minute growth velocity of just a few nanometers per minute.

2.5. Laser Ablation

Silicon nanowire growth via laser ablation differs in many respects from the nanowire growth techniques discussed so far. The two major differences are that (A), unlike growth via CVD or MBE, the catalyst material is coablated together with Si and (B) silicon nanowire growth does at least partially take place already in the vapor phase.

This is illustrated in Figure 7a. Typically, experiments are performed in a tube furnace into which the laser ablation target is placed. Morales and Lieber,[66] who pioneered this nanowire synthesis method, used a mixed Si−Fe target containing about 90% Si and 10% Fe. They heated the tube furnace to a temperature of 1200 °C, which is close to the minimum temperature required for Fe-catalyzed VLS Si nanowire growth. A constant Ar flow of 500 sccm was directed through the furnace, held at a pressure of 500 Torr. Under these conditions, they ablated Fe and Si from the laser target by shooting at it with a pulsed, frequency doubled Nd:YAG laser (wavelength 532 nm).[66] The ablated material collides with inert gas molecules and condenses in the gas phase, resulting in Fe−Si nanodroplets, which act as seeds for VLS Si nanowire growth. Zhang et al.[67] reported nanowire growth velocities on the order of micrometers per minute. The nanowires are harvested at the downstream end of the tube. The thus obtained Si nanowires had a crystalline core of less than 10 nm in diameter and were covered by an amorphous shell of 5 nm thickness, with the preferential growth direction being ⟨111⟩ .[66]

Similar experiments were performed by other groups,[67−69] and a typical example of Si nanowires obtained by laser ablation is shown in Figure 7b. Peng et al.[69] investigated the influence of temperature, Zhang et al.[70] the influence of ambient gas, and Zhou et al.[71] the crystallography of the nanowires. As an alternative to Fe, also Ni,[72] Pr,[73] and Ru[73] were successfully tested as catalyst metals. Most interestingly, also the addition of SiO_2 to the laser ablation target served the purpose well.[74,75] What is remarkable about this oxide-assisted growth[76] is that SiO_2 containing targets clearly increased the Si nanowire yield compared to pure silicon targets or mixed silicon−metal targets.[72] If growth is carried out with an SiO_2 containing target, the preferential growth directions are ⟨112⟩ and ⟨110⟩,[73,76,77] but Zhang et al.[76] also report to have found pentagon-shaped, ⟨100⟩ oriented Si nanowires. This is interesting, because thin Si nanowires with a regular, pentagon-shaped cross section have been proposed by theory to be energetically favorable structures.[78] Unfortunately, the experimentally observed pentagon-shaped nanowires do not appear to be regularly pentagon-shaped but rather square-shaped with one corner diagonally cut off.[79]

The advantages of laser ablation as a Si nanowire growth technique are mainly technical simplicity and versatility: technical simplicity, because there is no need for sophisticated gas installations; versatility, because the composition of the nanowires can be varied by simply changing the composition of the laser ablation target. Tang et al.,[80] for example, produced phosphorus doped Si nanowires by means of laser ablation. By combining silane CVD with laser ablation, Cui et al.[81] managed to synthesize p- and n-doped Si nanowires. Another advantage is that due to the high temperatures generated, also nongold catalyst materials such as Fe can be used. The main disadvantage of laser ablation is that it is not the right method for an in-place epitaxial growth of silicon nanowires.

2.6. Silicon Monoxide Evaporation

A cost-effective method to produce Si nanowires is silicon monoxide, SiO, evaporation. For this, a simple tube furnace connected to an inert gas supply can be used, as indicated in Figure 8a. For the successful nanowire synthesis, it is important that the tube furnace exhibits a temperature gradient and that the inert gas flows from the hotter to the colder part of the furnace. Some amount of SiO is then placed in the hotter zone, where it evaporates. The evaporated SiO is carried away by the gas stream to the cooler end of the tube, where it undergoes a disproportionation reaction into Si and SiO_2, thereby forming the nanowires.[82] Due to the disproportionation reaction, the Si nanowires are covered by a thick SiO_x shell (see Figure 8b), with x having a value between 1.5 and 2.[82] Another implication of the disproportionation reaction is that the diameter ratio between crystalline core and amorphous shell remains approximately constant.[83] Typical growth parameters involve pressures in the 100 Torr range, flow rates of 50 sccm of inert gas or an inert gas hydrogen mixture, temperatures of 1100−1350 °C for SiO evaporation, and temperatures of 900−1000 °C for Si nanowire growth.[83−86]

With SiO evaporation, two different growth modes are possible: growth with and without metal catalyst. Growth without catalyst[82,85−87] works via the aforementioned oxide assisted growth mode and presumably involves a liquid SiO_x phase at the nanowire tip.[76] For this mode, ⟨111⟩ and ⟨112⟩ growth directions have been reported. Metal catalyzed growth

via the VLS mechanism has been demonstrated for Au.[83,84] In contrast to the normal VLS mechanism, however, the interaction between the droplet and the nanowire is far more complex, because not only the growth of the crystalline Si core but also the growth of the SiO_x shell has to be considered. Therefore, it is not too astonishing that this more complex growth mechanism also leads to more complex phenomena, such as the periodic instability observed by Kolb et al.[84] They found that Au-catalyzed Si−SiO_x core−shell nanowires exhibit nicely regular diameter oscillations with the oscillations of core and shell being slightly phase shifted with respect to each other.

The main disadvantage of Si nanowire growth via SiO evaporation is clearly its lack of controllability of nanowire diameters and lengths. Also, a controlled doping of the nanowires seems difficult. Another main drawback is that epitaxial growth on Si substrates is impossible, as the substrate would oxidize rapidly under the prevailing oxygen-rich conditions. The main advantage is clearly its technical simplicity, as a tube furnace is the only equipment required. Together with the solution based approach, Si nanowire growth via SiO evaporation presumably represents the most cost-efficient way of producing Si nanowires.

3. Catalyst Materials

Au has been the catalyst material of choice for Si wire growth ever since the early publications of Wagner and Ellis.[2] It is instructive to take a closer look at the Au−Si system and try to figure out what it is that makes Au such a favorable catalyst material, because it provides some valuable insight into the criteria for catalyst metals in general.

3.1. Gold as Catalyst

From a purely practical point of view, many reasons favor the use of Au as catalyst material. The first is availability. Gold is one of the standard metals used in solid state research. Evaporation systems equipped with Au can presumably be found in most semiconductor research laboratories, so that depositing a thin layer of Au onto a sample is usually not a major obstacle. Alternatively to a thin evaporated layer, one can also use Au colloid nanoparticles, which are commercially available with diameters ranging from 2 to 250 nm.[88] Another advantage of Au is its high chemical stability. Although seemingly trivial, the fact that the Au does not oxidize in air is a decisive advantage for the pregrowth sample preparation, as it makes an in situ deposition unnecessary. The high chemical stability of Au furthermore reduces the technical requirements on the growth system, especially in view of the tolerable oxygen background pressure. The final practical advantage of Au is that Au is nontoxic, which is convenient from a work safety point of view.

The main reason why Au is used for Si wire growth, however, lies in its binary phase diagram with Si, shown in Figure 9a. One can see that the Au−Si phase diagram is of the simple eutectic type, with its dominant feature being a eutectic point at a composition of about 19 atom % Si and a temperature of 363 °C. The eutectic temperature is about 700 K lower than the melting point of pure Au and about 1050 K below the melting point of pure Si, which signifies a quite remarkable reduction of melting temperature. The phase within the V-shaped region, visible in Figure 9a, is the liquid phase, the actual composition of which depends

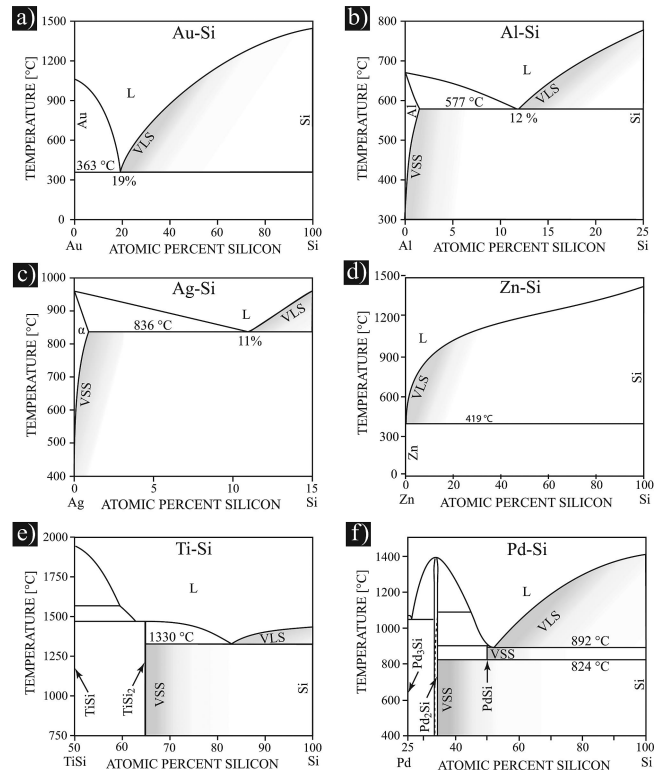


Figure 9. Schematic phase diagrams of different metal−Si systems. (a) Au−Si, (b) Al−Si, (c) Ag−Si, (d) Zn−Si, (e) Ti−Si, (f) Pd−Si.[121,123] After Schmidt et al.[4] The types refer to the classifications given in Figure 10.

on the amount of Si supplied. For Au−Si alloy droplets on a Si substrate, Si is abundant, and the composition of such Au−Si droplets is therefore given by the position of the liquidus line on the Si side, i.e. the phase boundary on the right-hand side (rhs) of the liquid phase. If such Au−Si droplets on a Si substrate, held at temperatures above the eutectic temperature, are exposed to a Si precursor such as silane, SiH_4, silane molecules will crack at the surface of the droplets, thereby supplying additional Si to the droplet. This additional Si supply causes an increase of the Si concentration in the droplet to a value greater than the equilibrium concentration. Considering the Au−Si phase diagram shown in Figure 9a, this means that, by switching on the silane, the Au−Si droplet system is pushed over the liquidus line; and the only way for the droplet to reduce the Si concentration is to precipitate a Si-rich solid. In general, the composition of such a Si-rich solid would be given by the nearest phase boundary on the Si side of the liquidus. In the Au−Si case, the Si-rich solid happens to be pure Si. Consequently, the droplet precipitates Si, which with time results in the growth of a wire.

To formulate the requirement on the catalyst−Si binary phase diagram in a more abstract way, Si wire growth requires a nonhorizontal phase boundary over which one can push the catalyst−Si system to enforce the precipitation of a Si rich solid. Since we are interested in the growth of Si wires, the Si-rich solid needs to be Si itself, which means that the phase boundary over which to push the catalyst−Si system has to adjoin the pure Si side of the phase diagram. In the case of the VLS growth mode, this phase boundary is a liquidus line, as in Figure 9a. But this is not a necessary condition. For VSS Si wire growth, that is, growth via a solid catalyst particle, the phase boundary in question can also be a phase boundary limiting the Si solubility in the

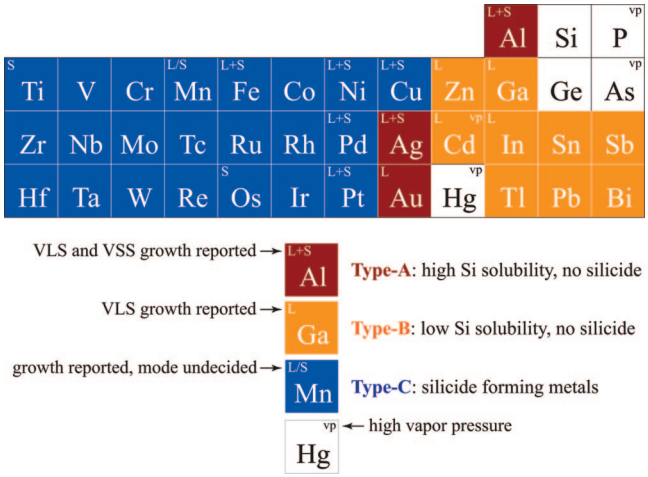


Figure 10. Periodic table with potential catalyst metals classified according to their phase diagram. Type-A: phase diagram dominated by a eutectic point at a Si concentration > 10%; no metal−silicide phase present. Type-B: phase diagram dominated by a eutectic point at a Si concentration < 1%; no metal−silicide phases present. Type-C: phase diagram with one or more metal−silicide phases; eutectic points located at temperatures above 800 °C. Elements marked with superscript vp have a vapor pressure of more than 0.01 mbar at 300 °C.

solid catalyst material itself, such as the Al pocket on the left-hand side (lhs) of Figure 9b, or it can as well be a silicide phase, such as the $TiSi_2$ phase shown in Figure 9e. According to what was stated above, namely that the phase boundary required for Si wire growth has to neighbor the pure Si of the phase diagram, one can expect the most Si-rich silicide phase to be present during VSS Si wire growth. We will see later on that this indeed turns out to be the case.

Another quite important feature of the Au−Si binary phase diagram (see Figure 9a) is its relatively high Si concentration of about 19 atom % at the eutectic point. Si apparently likes to mix with Au. Consequently, the energetic costs per Si atom of increasing the Si concentration beyond its equilibrium value can be expected to be small. This can also be seen from the moderate slope of the liquidus line near the eutectic. As a consequence, the Si pressure required to achieve a certain increase of the Si concentration can be expected to be lower for liquids with a high equilibrium solubility of Si than for those with low equilibrium solubility. Expressed differently, catalyst metals with low Si solubility such as In or Ga, presumably require higher precursor pressures than Au. For completeness, it must be mentioned here that the large Si solubility may also turn into a disadvantage regarding the synthesis of axial nanowire heterostructures, as discussed in section 5.

One important property of Au is its conveniently low vapor pressure, even at high temperatures. At temperatures below about 800 °C, the vapor pressure of Au is smaller than 10^{-8} mbar, and evaporation of Au is not an issue under usual Si wire growth conditions. We will see later on that some potential catalyst materials can be excluded just because of their high vapor pressure. Hg with a vapor pressure greater than 1 mbar at 400 K is one example. One aspect that has not been addressed so far concerns the surface tension of the liquid Au−Si alloy. According to the surface tension criterion, discussed in section 8, a certain minimum value of the droplet surface tension is required for wire growth. This criterion is well met by the Au−Si alloy.

In summary, the main advantages that make Au such a favorable catalyst material are that it is nontoxic, chemically stable, and readily available; that it possesses a low temperature eutectic with comparably high Si solubility; that it has a low vapor pressure at elevated temperatures; and that the Au−Si liquid alloy has a high enough surface tension. Unfortunately, these advantages are balanced by one serious drawback, which is that Au, known to contaminate the nanowires,[89−91] is very much disliked by the semiconductor industry, because it is associated with deep-level defects in Si, leading to strongly enhanced carrier recombination.

3.2. Alternative Catalyst Materials

In view of the incompatibility of Au with complementary metal-oxide-semiconductor (CMOS) production standards, strong efforts have been made in the past to identify an alternative, non-Au catalyst material for Si wire growth. Metal impurities in semiconductors are generally known to affect the charge carrier lifetimes by facilitating charge carrier recombination. The maximal recombination rate associated with a particular metal impurity, however, strongly depends on the energetic positioning of the corresponding impurity level within the band gap of the semiconductor. To be more precise, the recombination rate critically depends on the energy difference between the impurity level or levels and the band gap middle; the closer the impurity level is to the band gap middle, the more efficient it is as a recombination center. The use of metals with impurity levels close to the band gap middle, so-called deep levels, is therefore to be avoided. Concerning the use of Au, the problem is further exacerbated by the high chemical stability of Au that makes a cleaning of Au contaminated samples or Au contaminated equipment difficult, to say the least.

A large variety of catalyst materials have been tested for their ability to replace Au. Those metals for which successful Si wire synthesis is reported in the literature are as follows: Ag,[2,11,14,16,30,92,93] Al,[40,93−99] Bi,[57,100] Cd,[14] Co,[55] Cu,[2,7,11,14,16,30,56,89,93,101,102] Dy,[3] Fe,[3,66−69,72,103−106] Ga,[37,39,93,99,107] Gd,[14] In,[40,93,100,107,108] Mg,[14] Mn,[14] Ni,[2,10,11,14−16,30,55,72,93,109−111] Os,[14] Pb,[100] Pd,[2,10,14,30,35,93] Pr,[73] Pt,[2,6,10,11,16,93,112,113] Ru,[73] Sn,[114] Te,[100] Ti,[115−117] and Zn.[13,93,100,118]

As one can see, the number of possible catalyst materials is quite large. Although the quality of the wires obtained as well as the required growth conditions differ strongly, there are also similarities in the behavior of the different catalysts. In order to discuss the differences and similarities in a concise manner, it is useful to classify the catalyst materials with respect to the characteristics of their corresponding metal−Si binary phase diagrams. We will adopt here the classification scheme similarly introduced by Bootsma et al.[30] The catalyst materials are classified into three different categories: type-A, type-B, and type-C, as shown in Figure 10.

Type-A catalysts are the Au-like metals. Their phase diagram is of the simple eutectic type; that is, it is dominated by a single eutectic point. This eutectic point is located at a Si composition of more than 10 atom % Si. Furthermore, type-A catalysts do not possess any metal−silicide phases. There are only three type-A metals: Al, Ag, and Au.

Type-B catalysts are the low Si solubility metals. Their phase diagrams also show a single dominant eutectic point but no silicide phases. In contrast to the type-A catalysts, the eutectic point is located at much lower Si concentrations, less than 1 atom % Si. Typical type-B catalysts are In, Ga, or Zn.

Type-C catalysts are the silicide forming metals. Their phase diagram indicates the presence of one or more silicide

phases. In addition, the lowest eutectic temperature is higher than 800 °C. Typical type-C catalysts are Cu, Pt, or Ti.

3.2.1. Type-A, Au-like Catalysts

Among the various catalyst materials, Al is the one whose Si binary phase diagram (see Figure 9b) shows the closest similarity with Au−Si. Though the eutectic point of the Al−Si system is located at a higher temperature (577 °C) and at a slightly lower Si concentration (12 atom %), the Al−Si and Au−Si phase diagrams are very much alike. With the phase diagrams being so similar, it is not too astonishing that VLS growth can be performed with Al as catalyst. Osada et al.[94] demonstrated Al catalyzed VLS growth of crystalline Si wires in a CVD process using silane and applying temperatures of 580−700 °C. Al-catalyzed Si nanowire growth under comparable conditions was also reported by Whang et al.[96−98] The authors claim to have grown Si nanowires at 540 °C via the VLS mechanism. This at first seems inconsistent, as the growth temperature reported by them is about 40 K below the eutectic temperature of the bulk Al−Si system. Even considering the surface-induced reduction of the eutectic temperature (see section 6), one may ask whether these wires actually grew in the VSS rather than the VLS growth mode. This is supported by the fact that Wang et al.[95] demonstrated the synthesis of well shaped, single crystalline, Al-catalyzed Si nanowires grown epitaxially on Si(111) substrates at a growth temperature of 430−490 °C; see Figure 3b. Since this growth temperature was well below the Al−Si eutectic point, Wang et al.[95] concluded that Si nanowires grew via the VSS mechanism, though this conclusion has recently been questioned.[119] Wang et al. point out that Al-catalyzed VSS growth is related to a peculiarity of the Al−Si phase diagram, not present in the Au−Si phase diagram, namely the pocket on the lhs of Figure 9b. This pocket indicates that up to about 1 atom % Si can be dissolved in solid Al at temperatures of 500 °C. The phase boundary limiting the Si solubility in solid Al is adjoining the pure Si side of the phase diagram. Therefore, all requirements for Si wire growth are fulfilled. By supplying a sufficient Si pressure, this phase boundary can be used to induce the precipitation of solid Si, that is, the growth of Si wires.

Synthesis via a solid Al particle brings the advantage that the solubility of Si in the catalyst particle is about 1 order of magnitude smaller than the eutectic composition. This low solubility, though potentially slowing down the growth process, could be beneficial for the fabrication of axial Si−Ge heterostructures with sharp transitions. As will be discussed in section 5, axial Au-catalyzed Si−Ge heterostructure nanowires do not show sharp transitions between Si and Ge, because of the high solubility of Si or Ge in the Au catalyst droplet. With lower solubility in the catalyst droplet or particle, sharper transitions between Si and Ge should be achievable. The use of Al, however, has another important advantage. Al does not create deep level defects. On the contrary, the position of the impurity level (see Figure 11) shows that Al is a p-type dopant, and one can therefore expect the nanowires to be strongly p-doped. A comparison with Al solid phase epitaxy experiments implies an Al doping of 10^{18} to 10^{19} cm^{-3}.[120] Whether p-type doping is an advantage or not is difficult to decide, but having the possibility to directly synthesize highly p-doped wires, without the need of a vapor-phase dopant, is at least a potentially useful feature. The major drawback of the use of

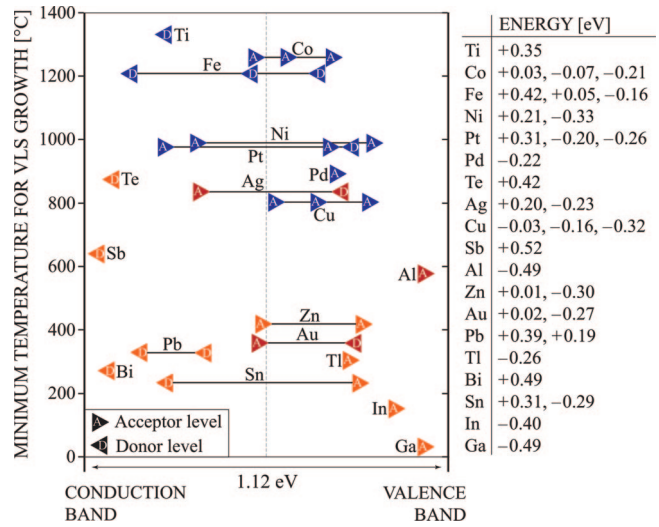


Figure 11. Minimum temperature of certain metals required for vapor−liquid−solid (VLS) growth of Si nanowires plotted versus their respective impurity level energies in Si[193] after ref 4. The energies of these impurity levels are given on the rhs with respect to the middle of the band gap (assuming a band gap of Si of 1.12 eV). The color code refers to the catalyst classification of Figure 10: red, type-A; orange, type-B; blue, type-C.

Al, however, is its oxygen sensitivity. Oxidation of the Al catalyst particle has to be prevented during the whole processing sequence, which clearly limits the usability of Al.

Silver is the second nongold, type-A catalyst. Like Au, the Ag−Si system (see Figure 9c) possesses a single eutectic point (at 11 atom % Si and 836 °C).[121] Due to the high eutectic temperature, high process temperatures are required for Ag-catalyzed VLS growth of Si wires. Wagner and Ellis[16] reported VLS growth of single crystalline Ag-catalyzed Si wires by a $SiCl_4$CVD process at temperatures of 950−1050 °C. That VLS growth under such conditions is indeed possible has been confirmed by Nebolsin et al.,[11] who managed to grow Si wires at a growth rate of about 1.5 μm/s in a similar process. What is astonishing about these results is that the catalyst material did not evaporate completely under these conditions, as the vapor pressure of Ag reaches a value close to 10^{-2} mbar at 1000 °C, which is about 3 orders of magnitude larger than that of Au.[122]

Regarding the use of Ag, it is interesting that Tatsumi et al.[92] claim to have synthesized amorphous Si wires by a silane CVD process at 650 °C, that is, well below the eutectic temperature, indicating VSS growth. This seems surprising, as most Ag−Si phase diagrams (see, for example, ref 123) do not show any significant solubility of Si in solid Ag, and wire growth experience suggests that a certain solubility of Si is necessary. This problem, however, has recently been resolved by a reevaluation of the Ag−Si phase diagram,[121] which revealed that the solid solubility of Si in Ag is about 0.2 atom % at 650 °C and 0.9 atom % close to the eutectic temperature, as shown in Figure 9c. The Ag−Si phase diagram thus resembles the Al−Si phase diagram, except that the eutectic point is located at higher temperatures and that the pocket on the lhs is less pronounced. Consequently, VSS Si nanowire growth with Ag as catalyst seems possible, and in view of the excellent results that have been obtained with Al as catalyst, Ag-catalyzed VSS growth seems very promising; particularly as the impurity levels of Ag (see Figure 11) are well positioned, being neither too close to

the band gap center nor to the conduction or valence band. Initial experiments on Ag-catalyzed VSS growth of silicon nanowires have been performed in our group.

3.2.2. Type-B, Low Si Solubility Catalysts

The type-B catalysts are characterized by a eutectic point at very small Si concentrations. Let us first look at the transition metals Zn and Cd. The Zn−Si binary phase diagram is dominated by a single eutectic point at 420 °C and 0.02 atom % Si, shown in Figure 9d, and despite its high vapor pressure of 0.2 mbar at 420 °C, Zn has proven to be an effective catalyst material for VLS growth. Chung, Yu, and Heath[13,118] demonstrated VLS Si nanowire growth by a silane CVD process at temperatures of 440−500 °C. They managed to synthesize Si nanowires with diameters between 15 and 35 nm and observed both ⟨111⟩ and ⟨211⟩ oriented nanowires, with the ⟨211⟩ oriented nanowires being virtually defect-free.[118] In view of the electronic properties, however, one must conclude that the impurity levels of Zn in Si (see Figure 11) are basically as detrimental as those of Au. The only real advantage of using Zn is that a potential Zn contamination of wafers or equipment can be removed more easily than a potential Au contamination.

Little is known on the use of Cd as catalyst, except for the remark that "cadmium promoted whisker growth when the source material was arsenic-doped silicon".[14] The phase diagram (eutectic at 321 °C and 0.14 atom % Si) strongly resembles that of Zn. Thus, Cd-catalyzed Si wire growth via the VLS mechanism could be possible, if one manages to prevent a complete evaporation of the catalyst material during growth. The Cd vapor pressure (greater than 1 mbar at 321 °C) is even higher than that of Zn, and this high vapor pressure is the main limitation for the use of Cd as catalyst material.

The use of Ga or In appears to be much more attractive than that of Zn or Cd from a vapor pressure point of view. At 500 °C, the vapor pressure of In is below 10^{-7} mbar, and the vapor pressure of Ga is even lower: 10^{-10} mbar. Moreover, In and Ga would also be attractive from an electronics point, as both would induce a p-type doping of the wires (see Figure 11). In terms of phase diagrams, Ga and In show great similarities. The Si concentrations at the eutectic point (smaller 0.01 atom %) as well as the eutectic temperatures (Ga, 30 °C; In, 156 °C) are very low in both cases, and any reasonable CVD growth temperatures will be way above the respective eutectic temperature. One can therefore expect In or Ga to produce similar results, a fact that has been experimentally confirmed by Givargizov et al.[107] They synthesized conical Si wires using In and Ga at high temperatures (900−1050 °C) using $SiCl_4$. The authors attributed the conical shape to the incorporation and/or evaporation of the catalyst material.[107] More recently, Iacopi et al.[40,108] and Sharma et al.[39] using In and Ga, respectively, demonstrated Si nanowire synthesis by plasma-enhanced chemical vapor deposition (PECVD) at temperatures of 500−600 °C using silane as Si precursor.

Only little information exists on Si wire growth with other type-B catalysts, such as Tl, Sn, Pb, Sb, and Bi. Miyamoto et al.[100] reported amorphous Si fibers at temperatures of 500−600 °C using Bi and Pb as catalysts. The eutectic temperatures of Pb and Bi are 328 and 271 °C, respectively. VLS growth therefore seems likely. According to Nebolsin et al.,[93] the surface tensions of liquid Sn, Pb, Sb, or Bi are too small for stable wire growth, as discussed in detail in section 8. In the case of Bi, for example, it is unclear whether indeed the too low surface tension or the too low Si solubility hinders nanowire growth under conditions comparable to the ones used for Au as catalyst. As mentioned in subsection 3.1, it could be that one simply has to apply higher Si partial pressures to realize wire growth with type-B catalysts. Both the fact that plasma assistance was necessary in order to obtain In- or Ga-catalyzed wires as well as the fact that solubility and growth velocity are correlated[11] would support such an assumption. This would also fit with recent results of Heitsch et al.,[57] who managed to synthesize Bi-catalyzed Si nanowires using trisilane, which is very reactive, as a precursor. Even if the assumption that lower Si solubility means higher minimum partial pressures is taken for granted, the question whether it is the solubility itself or the surface tension that causes the problems remains undecided, as the surface tension somehow correlates with the Si solubility. There is definitively a need for clarifying experimental and theoretical investigations, especially since the use of Bi, Tl, and Sn as catalyst would be quite attractive from an electronics point of view (see Figure 11).

3.2.3. Type-C, Silicide Forming Catalysts

Type-C catalysts are the silicide forming catalyst metals. The phase diagrams of type-C catalysts are typically rather complex, exhibiting several silicide phases and various eutectic points. Due to the presence of silicide phases, the type-C catalyst can be used not only for VLS but also for VSS wire growth via the silicide particle. This shall be discussed here considering Si nanowire growth based on Ti.[39,115,116] Figure 9e schematically depicts the Si-rich half of the Ti−Si phase diagram. As indicated therein, Ti−Si possesses a eutectic point at 1330 °C adjoining the pure Si side of the phase diagram, whose liquidus can be used for Si wire growth via the VLS mechanism. At growth temperatures below 1330 °C, growth should theoretically proceed via the phase that at this temperature is neighboring the pure Si side. As one can see in Figure 9f, this would be $TiSi_2$. Considering growth at 1000 °C and starting from a Ti particle, this Ti particle will first transform into Ti_5Si_3 and then into Ti_5Si_4, which becomes TiSi, which will finally transform into $TiSi_2$. Only once this transformation process is complete can Si wire growth start. $TiSi_2$-catalyzed, VSS Si nanowire growth has first been demonstrated by Kamins et al.,[115] who synthesized Si nanowires at 640−670 °C by means of a CVD process. The main advantages of Ti are its favorably positioned impurity level (see Figure 11) and its low solubility in Si. Ti is assumed to be compatible with CMOS technology. The crystallographic quality of Si nanowires grown via a $TiSi_2$ catalyst particle, however, seems to be rather poor compared to what can be obtained by using Au as catalyst.

The use of Fe or Dy as catalysts in CVD processes at temperatures around 600 °C leads to similar growth results as for Ti, in the sense that the Si nanowires show a high density of crystallographic defects.[3] It appears to be a general trend that nanowires grown via a silicide particle tend to have a higher density of crystallographic defects than VLS-grown ones. This finding is indirectly supported by the results of Morales et al.,[66] who grew nanowires of high crystalline quality using Fe as catalyst; but they used laser ablation from a mixed Fe−Si target and applied temperatures of about 1200 °C, which is close to the melting point of the Fe−Si alloy. Thus, one can assume that their nanowires grew via the VLS

mechanism, with no silicide phase present, which would explain the good crystalline quality.

Other type-C catalysts are the noble metals Pd and Pt, which are known to have similar physical and chemical properties. According to their binary phase diagrams, both Pd (see Figure 9f) and Pt would require high temperatures for VLS growth (Pd, 892 °C; Pt, 979 °C). At such high temperatures, results similar to those obtained with Au as catalyst can been obtained.[2] This can best be seen in the work of Weyher[112] and Wagner et al.,[16] who both synthesized Pt-catalyzed VLS grown Si wires by $SiCl_4$ CVD at temperatures around 1000 °C; and both obtained ⟨111⟩ oriented wires with hexagonal cross sections and {211} side facets. A very interesting result has been reported by Bootsma et al.,[30] who stated therein that "Filamentary growth was also obtained with Ag, Cu, Ni and Pd at substrate temperatures of about 800 °C". This is surprising as each of these metals requires temperatures of more than 800 °C for VLS Si wire growth (see Figure 11). In the case of Pd, the reported growth temperature is almost 100 K below the minimum temperature required for VLS growth. Of course, one has to consider the possibility that the catalyst particle is in a metastable undercooled state, so that despite the low temperature, growth could possibly still proceed via the VLS mechanism. Growth via the VSS mechanism, employing a solid silicide particle, however, could provide another plausible explanation. The Pd−Si phase diagram shown in Figure 9f indicates that VSS growth at 824−892 °C would be mediated by a PdSi silicide particle. At temperatures below 824 °C, VSS growth should be catalyzed by a Pd_2 Si particle. This has recently been confirmed by Hofmann et al.,[35] who performed in situ transmission electron microscopy (TEM) studies on Pd-silicide catalyzed Si nanowire growth. Hofmann et al.,[35] applying growth temperatures of 892 °C, furthermore found that the nanowires grow via lateral ledge flow at the Si−silicide interface. With regard to possible silicides, the situation for Pt is less complex than that for Pd. According to the Pt−Si phase diagram, growth at temperatures below 979 °C should proceed via a solid PtSi particle, which has been confirmed by Baron et al.[113] Similar results have also been obtained by Garnett et al.[6]

Both, Cu and Ni are very attractive catalyst materials, but for different reasons. Although Cu, like Au is a very efficient recombination center in Si, it is attractive because Cu is already used for interconnects in integrated circuits (ICs); so one cannot argue that Cu is totally incompatible with CMOS technology. Ni on the other hand is attractive because of its favorable impurity levels in Si (see Figure 11) and because Ni-silicide is used for electrical contacts in well-known standard technologies. The minimum temperature required for Ni VLS Si wire growth is 993 °C, which is about 200 K higher than that of Cu (802 °C); and at these comparably high temperatures, both Cu and Ni produce Si wires of similar quality to Au.[14,16] In the case of Cu, this has recently been demonstrated by Kayes et al.;[7] see Figure 2b. They synthesized arrays of perfectly aligned, ⟨111⟩ oriented Si wires using Cu as catalyst in a $SiCl_4$CVD process at temperatures of 850−1100 °C. For Cu also, VSS growth has been demonstrated. Yao et al.[101] grew ⟨111⟩ Si nanowires at 500 °C via the VSS growth mode, and in accordance with the Cu−Si phase diagram, they found a Cu_3Si silicide particle at the tip of the nanowires. The Si nanowires obtained, however, showed a significant number of crystallographic defects. Similar results were obtained by Arbiol et al.[102]

To summarize this section, the type-C catalysts work well, but only in the VLS growth mode, i.e. at high temperatures. At lower temperatures, where silicide-catalyzed VSS growth prevails, problems with the crystalline quality of the wires arise. The type-B catalysts such as In and Ga work, but only under rather harsh experimental conditions. Compared to In or Ga, growth using Zn seems to be easier, but there is no big advantage of Zn compared to Au, except for the contamination removal. Thus, in the end, for low-temperature processes, everything boils down again to the use of the three type-A catalysts, Al, Au, and possibly Ag.

4. Crystallography

VLS grown silicon nanowires are in most cases highly crystalline diamond-type crystal structures. Aiming at an in-place epitaxial growth of Si nanowires on Si substrates, one typically wants to control the nanowire position and diameter and—seemingly most challenging—also the crystallographic growth direction of the nanowires. Growing nanowires with well-defined crystallographic orientations is not only important for an in-place growth of Si nanowires, where random growth directions are not what is intended. Since the physical and particularly the electrical properties of Si depend on the crystallographic orientation, control of the nanowire growth direction would be advantageous.

Considering epitaxial in-place growth of silicon nanowires on Si substrates, one faces two problems related to the crystallographic orientation of the nanowires. And these two problems should be clearly distinguished. The first concerns the question as to which family of growth directions the nanowires belong. This question can be answered, for instance, by breaking the wires off the substrate and investigating them by transmission electron microscopy. Typically, only three families of growth directions are observed; these are ⟨110⟩, ⟨112⟩, and ⟨111⟩ .[1,16,26,27,76,79,124] With few exceptions,[16,48,50,76,79,113] this observation holds for Si nanowire growth in general and, interestingly, is almost independent of the growth method employed. The observation that Si nanowires are typically ⟨111⟩, ⟨110⟩, or ⟨112⟩ oriented does, of course, not rule out that one or the other of these three families is favored by the specific growth conditions, such as, for example, ⟨111⟩ for wires of large diameter.

For CVD grown Si nanowires, it has been observed that the nanowire growth direction shows a marked diameter dependence.[26,27] Nanowires with diameters less than about 20 nm prefer to grow in ⟨110⟩ directions, whereas thicker Si nanowires with diameters larger than about 50 nm favor the ⟨111⟩ orientation. In addition, there exists a certain probability that ⟨112⟩ nanowires can be found;, with the probability for this being maximal in the transition region between 20 and 50 nm.[26,27] This change of growth direction can presumably be attributed to the scaling behavior of different energetic contributions: the contribution of the side faces, being proportional to the diameter d, versus the contribution of the liquid−solid interface and the Si volume, being proportional to d^2.[26,27] One can argue that, due to this difference in scaling behavior, thin Si nanowires rather tend to choose an orientation that provides energetically favorable side faces, whereas thick Si nanowires choose the orientation that minimizes the contribution of the wire−catalyst interface.

Nonetheless, even if growth conditions can be adjusted such that only one specific family of directions, e.g. ⟨111⟩, is preferred, one still faces the problem that there is usually

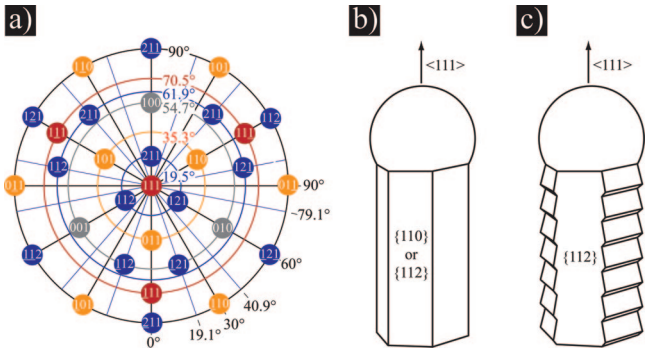


Figure 12. (a) Stereographic projection with respect to the [111] orientation. The degrees on the circles indicate the inclination angle with respect to the [111] direction. The degrees at the perimeter correspond to the azimuth angle. (b) Hexagonal nanowire. (c) Sawtooth faceting after Ross et al.[33]

more than one member to the family. Considering epitaxial nanowire growth, this leaves multiple orientations for the nanowire to choose from. For clarity, a stereographic projection indicating the orientation of the members of the three major families of growth directions with respect to the [111] direction is shown in Figure 12a. The further apart the spots in Figure 12a are from the 111 center spot, the more the growth direction would be tilted relative to an imaginary [111] substrate normal. Considering for instance the ⟨111⟩ family, one can see that in addition to the perpendicular [111] direction there are also three other possible ⟨111⟩ directions, which are inclined by an angle of 70.5° with respect to the [111] direction. Thus, even if ⟨111⟩ growth is ensured, some wires might still choose one or the other of the inclined ⟨111⟩ directions. This particular scenario was investigated in detail by Schmid et al.,[29] who found that the percentage of nanowires with diameters of 75 nm that grow perpendicular on a (111) substrate can be increased to about two-thirds if low growth temperatures (480 °C) and low silane partial pressures (80 mTorr) are applied. The percentage of wires grown normal to the (111) substrate surface is generally larger for larger diameters, which can be intuitively understood by considering that a change of the growth direction also requires a tilt of the catalyst droplet in the initial phase of growth; and tilting the catalyst droplet becomes energetically more cost-intensive as the wire diameter becomes larger. A somehow related and often observed problem is that a good percentage of the Si wires tend to change their growth direction during growth; see Figure 1b. They are then said to be kinked.[45,46] The influence of silane partial pressure and growth temperature on kinking was investigated in detail by Westwater et al., who found that the application of higher growth temperatures and lower pressures reduces kinking.[46]

It is well-known that crystals like to have crystallographically defined surfaces, and as expected, this is also the case for Si nanowires. Especially at elevated temperatures, where surface diffusion is fast, Si wires show a pronounced faceting of the surface.[112] ⟨111⟩ oriented Si wires often show a hexagonal cross section with either {110} or {112} surface facets,[14,16,107,125] as sketched in Figure 12b. According to Ma et al.,[126] ⟨110⟩ oriented nanowires also have hexagonal cross sections with four {111} and two {100} facets.

Concerning surface facets, an interesting observation has been made by Ross et al.[33] By growing Si nanowires in situ in a transmission electron microscope and directly monitoring their growth, they found that Si nanowires can also exhibit what they call sawtooth faceting; see Figure 12c. The Si nanowires in question are [111] oriented; and imagining for a second the sawtooth facets to be absent, the nanowire would be hexagonal in shape bounded by six {112} faces. Now instead of being just flat {112} planes, three of the side surfaces are roughened in a regular, sawtooth-like manner; see Figure 12c. Ross et al.[33] found that the upward-facing plane of such a sawtooth makes an angle of 78.8° with respect to the [111] nanowire axis, whereas the downward-facing sawtooth facets show an angle of 113.3°. Although Ross et al.[33] did not specifically assign crystallographic planes to these sawtooth facets, one can speculate that the three upward-facing facets presumably correspond to the ($1\underline{1}1$), ($\underline{1}1\underline{1}$), and ($\underline{1}\underline{1}1$) planes; and the downward-facing facet are presumably the ($3\underline{1}1$), ($\underline{1}3\underline{1}$), and ($\underline{1}\underline{1}3$) planes. Such an assignment would imply angles of 80.0° and 109.5°, respectively.

Si nanowires grown via the VLS mechanism are to a large extent single crystalline. While this seems also to be the case for Si nanowires grown via a solid Al catalyst particle,[95] the crystal quality of Si nanowires grown via the VSS mechanism and a type-C catalyst is often poor.[3,116] Typically, these wires show a multitude of planar crystal defects. The occurrence of planar defects is, however, not limited to VSS grown Si nanowires. One defect that is frequently observed for ⟨112⟩ oriented Si nanowires is a {111} twin defect parallel to the growth axis.[14,127]

Concerning the type of crystal structure, one would naturally assume that Si nanowires, like bulk Si, would be diamond-like cubic crystals. Recently, however, two publications appeared, in which the authors (from the same group) claim to have found evidence for a wurtzite-type crystal structure in Si nanowires: Arbiol et al.[102] for Cu-catalyzed VSS grown Si nanowires; Fontcuberta i Morral et al.[128] for Au-catalyzed VLS grown Si nanowires. Finding silicon with a wurtzite structure is surprising, as the occurrence of wurtzite-type silicon is otherwise only observed in indentation experiments, where pressures in the GPa range are locally exerted onto a Si crystal.[129] In view of this, Fontcuberta i Morral et al.[128] argue that the Si surface stress can induce pressures of greater 10 GPa at a nanowire radius of 100 nm. This, however, would require surface stresses on the order of 10^3 N/m^{-3} orders of magnitude larger than what is usual for Si.[130−132] Their evidence for the occurrence of wurtzite-type Si is mainly, though not entirely, based on TEM observation, for which planar defects can be a potential source for misinterpretations.[133] What, however, speaks in favor of their observation is that also growth of Si nanotubes has been reported.[134−138] These nanotubes resemble multiwall carbon nanotubes in appearance and may possess a different crystal structure than that in bulk Si. To the best of our knowledge, however, neither the growth nor structure of Si nanotubes is fully understood yet.

5. Heterostructures

One of the singular advantages of bottom-up nanowire synthesis is that heterostructure nanowires can be produced. Two generic types of nanowire heterostructures can be envisaged—axial and radial nanowire heterostructures. Both offer attractive features, and both are challenging from a synthesis point of view, in particular when the synthesis of epitaxial heterostructures is targeted. The synthesis of epitaxial heterostructures becomes difficult when two materials are to be combined that possess a non-negligible lattice

misfit with respect to each other. Due to the lattice misfit, the crystal structures of both materials need to expand or shrink, respectively. The materials are then said to be strained, with the strain characterizing the relative expansion/shrinkage. The elastic properties of the material couple the strain to its corresponding thermodynamic counterpart, the stress, in units of GPa, with the product of stress and strain being proportional to the strain energy density. In order to minimize energy, strained materials tend to partially relax by either one or both of two basic mechanisms: surface roughening, in case a free surface exists in the vicinity of the heterostructure interface, and/or incorporation of dislocations.[139] Both effects are usually unwanted: the first because it changes the morphology in an undefined way; the second because dislocations are potentially detrimental to the electronic properties. Ideally one likes to have nonroughened, dislocation-free, epitaxial heterostructures.

This is where the nanowires are interesting, because nanowires can relieve a considerable part of the strain energy by an elastic deformation of the nanowire itself. This can best be understood by considering a strained axial nanowire heterostructure: for instance, a Ge nanowire segment epitaxially grown on top of a Si segment. The lattice constant of Ge is about 4% larger than that of Si. Taking the elastic properties of Si and Ge to be the same, one can expect the strain to be equally distributed between Si and Ge. Consequently, Si is expanded by 2% in the radial and circumferential directions, whereas Ge is correspondingly compressed by 2%. This, of course, only works if the material can freely adjust its size, which is the case for a nanowire that can quite freely expand or shrink in both the radial and axial directions. Compared to a thin Ge layer on a bulk Si substrate where the strain is fully concentrated in the layer, such expansion/shrinkage would reduce the strain energy density by a factor of 4. The second advantage of nanowire heterostructures is their small volume. If the nanowire diameter is decreased, then the total strain energy of a misfit-strained heterostructure will at some diameter not suffice anymore to induce nucleation of misfit dislocations. Thus, axial nanowire heterostructures should be dislocation free if they are thin enough. This has first been recognized by Ertekin et al.,[140] who elegantly showed that the maximally allowed misfit at which dislocation nucleation would set in increases with decreasing nanowire radius. According to his estimate, Si−Ge nanowire heterostructures should be dislocation free for diameters less than 40 nm. A further theoretical treatment of dislocations in axial nanowire heterostructures was published by Kästner et al.[141]

Axial Si−Ge heterostructures would be attractive from an electronics point of view, as the band gap of Ge is 0.46 eV smaller than the one of Si. Therefore, charge carriers would face a steeplechase when driven through the nanowire in the axial direction, similar to what has been demonstrated for III−V heterostructure nanowires.[142] Furthermore, axial Si−Ge heterostructure superlattices could possibly be attractive, because ultrathin Si−Ge superlattices under certain conditions are assumed to develop a direct band gap.[143]

In principle, axial Si−Ge nanowire heterostructures are easy to produce by CVD—one simply has to switch precursors; and indeed, the VLS growth of Si−Ge or Si−SiGe heterostructured nanowires has been demonstrated by different groups.[59,144−148] The earliest publication dates back to the 1970s.[107] Figure 13a is reprinted from work of Wu et al.,[144] who managed to synthesize Au-catalyzed Si−SiGe heterostructure nanowires by a hybrid CVD laser ablation approach. One disadvantage of such Au-catalyzed, VLS grown, Si−Ge heterostructure nanowires is that due to the relatively high solubility of Si and Ge in the catalyst droplet, no sharp transitions between Si and Ge can be obtained. At the eutectic temperature, the liquid catalyst droplets contains about 19 atom % of Si, with the Au−Ge eutectic being even more Ge rich. Thus, when the precursor is switched from, for example, silane to germane, GeH_4, the Si still dissolved in the droplet has first to be diluted out of the droplet in order to get a pure Ge wire segment. If one estimates that about five full droplet fillings are required to get the dissolved Si out of the droplet, one can easily deduce that this will result in a graded junction having a width that approximately corresponds to the nanowire diameter. This phenomenon has been investigated in detail by Clark et al.[148] and a composition mapping along the wire axis across two heterostructure junctions (Si−Ge and Ge−Si) is shown in Figure 13c. In this graph one can nicely see that the heterostructure interfaces are not sharp but are rather smeared out. From the fact that the width of the transition region scales with both the nanowire diameter and the solubility of the nanowire material in the catalyst droplet, one can deduce that two things can be done to increase the sharpness of the interfaces. The first is to use a catalyst material that has a low solubility of both Si and Ge. Al, for example, would be an attractive material in this respect. The second is to simply go to smaller wire diameters.

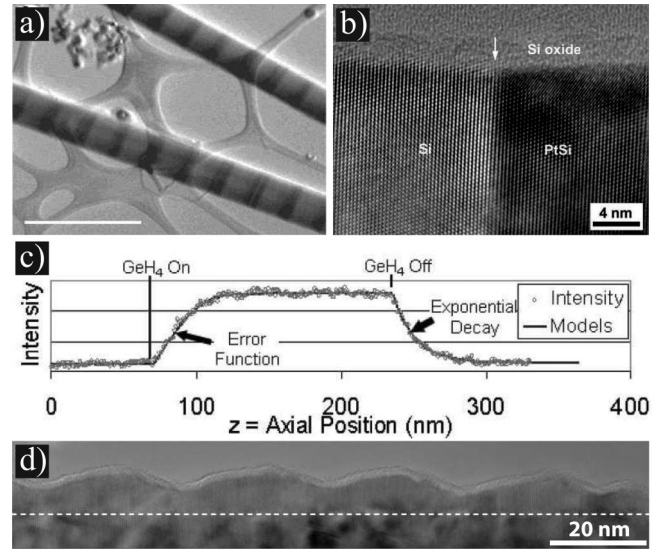


Figure 13. (a) Axial Si−SiGe heterostructure nanowires; scale bar is 500 nm. Reprinted with permission from Wu et al.[144] Copyright 2002 American Chemical Society. (b) Axial Si−PtSi nanowire heterostructure. Reprinted with permission from Lin et al.[161] Copyright 2008 American Chemical Society. (c) X-ray electron dispersive spectroscopy (XEDS). Intensity profile of an axial Si−SiGe−Si nanowire heterostructure measured along the nanowire axis. Reprinted with permission from Clark et al.[148] Copyright 2008 American Chemical Society. (d) Transmission electron micrograph of a radial Si shell grown on a Ge nanowire of 26 nm in diameter. Reprinted with permission from Goldthorpe et al.[150] Copyright 2008 American Chemical Society.

It was already mentioned that Si and Ge nanowire heterostructures are of potential interest for electronic applications. This not only holds for axial heterostructures but also for radial ones. In particular Ge-core−Si-shell radial heterostructures are attractive, since, due to the smaller band gap of Ge, charge carriers would be confined within the

heterostructure core.[149] This could potentially minimize surface scattering of charge carriers. In addition, a radial Ge-core−Si-shell heterostructure could be a remedy for the well-known problem that Ge does not possess a stable oxide. If a Ge-core is wrapped in a Si-shell, a stable SiO_2 coverage can be produced by simply oxidizing the wires.

Unfortunately, the synthesis of Ge-core−Si-shell nanowires is not trivial. When crystalline Si is deposited directly onto the Ge nanowire surface, a roughening of the nanowire surface can be observed, see Figure 13d.[150] This roughening is driven by the misfit strain. The theoretical origins of this roughening instability is well understood.[151−156] A different approach to Ge-core−Si-shell nanowire was pursued by Lauhon et al.[157] who deposited an amorphous Si-shell on crystalline Ge nanowires and recrystallized the shell by a subsequent thermal annealing step. In this way, a roughening of the shell can be circumvented, but, presumably, at the expense of having dislocations at the core−shell interface. Xiang et al.[158] demonstrated the fabrication of field effect transistors based on Ge-core−Si-shell nanowires produced that way.

Another innovative approach leading to nanowire heterostructures is a postgrowth alloying of Si nanowire segments with a properly chosen metal. This approach was pioneered by Wu et al.,[159] who deposited Ni on Si nanowires, which were then transformed by thermal annealing into single-crystalline NiSi nanowires. It is surprising at first view that silicide formation is not necessarily accompanied by a large volume expansion, but it is the case. Some metal silicides, such as CoSi and $CoSi_2$, for instance, only show minute volumetric changes compared to the original volume of Si; $CoSi_2$ formation is even accompanied by a slight shrinkage.[160] This small volumetric expansion of some metal-silicides allows for the fabrication of Si−metal-silicide heterostructures with crystallographically well-defined interfaces, as demonstrated for NiSi[159] and PtSi.[161] The advantage of this silicidation approach is that, assuming the metal is diffused into the nanowire from its ends in a controlled fashion, very thin Si segments sandwiched between the metal-silicide leads can be obtained.[161] These silicide segments are furthermore well suited for electrically contacting the Si segment, as silicidation is known to be an excellent method for obtaining low-ohmic electrical contacts. Weber et al.[162] demonstrated the feasibility of this approach by fabricating nanowire field effect transistors.

6. Surface Induced Lowering of the Eutectic Temperature

This section and the three subsequent sections deal with different aspects of the thermodynamics of silicon nanowire growth. Although the phenomena described in these sections are quite different in nature, they all have one thing in common; that is, they reflect how surfaces influence the growth of silicon nanowires. This could have been expected, as scaling down sizes of objects naturally comes with an increase of the surface-to-volume ratio. When dealing with nanoscale objects, the influence of surfaces can typically not be neglected.

One of the most prominent properties of surfaces is that they possess a specific surface free energy or surface tension. Customarily, the expressions surface free energy and surface tensions are used interchangeably, assuming that they are equal physical quantities. While this is indeed the case for liquids, it is generally not true for solids. This was first pointed out by Gibbs;[163] an excellent discussion on this matter was also given by Shuttleworth.[164] In order to avoid confusion, the term surface stress (a tensorial quantity) is conventionally used when dealing with solids. One can argue that the surface free energy of a solid is related to the work of creating new surface area, e.g. by splitting the material, whereas the surface stress is related to the work of increasing the surface area by elastically deforming the solid.[165] As we are not dealing with elastic properties of solids in this work, it is the surface free energy that matters for us. Following the conventionally interchangeable use of the terms surface tension and surface free energy, we will also speak of the surface tension of a solid, but what is meant by that is in fact its surface free energy.

As discussed in section 3, the question of whether silicon nanowire growth can be assumed to proceed via the vapor−liquid−solid (VLS) or the vapor−solid−solid (VSS) mechanism largely depends on the specifics of the respective metal−Si binary phase diagram. One should, however, be aware that binary phase diagrams are usually bulk phase diagrams, which means that the influence of surfaces is neglected. As mentioned above, such an assumption becomes problematic considering nanoscopic systems. In our context, probably the most important effect of surfaces on the characteristics of phase diagrams is that the eutectic points shift to lower temperatures. Following the work of Tanaka et al.,[166] the calculation of the shift of the eutectic temperature of a small spherical alloy droplet will be discussed in the following for the three type-A metal−Si systems: Au−Si, Ag−Si, and Al−Si. The calculation is actually rather simple and is presented here in detail.

As for most thermodynamic problems, one has to start with the thermodynamic potential. This is the Gibbs free energy, taken relative to the Gibbs free energy of the respective solid phases of the pure elements. The total Gibbs free energy ΔG_{tot} of a simple eutectic A−Si (A stands for Au, Al, or Ag) binary alloy can be assumed to consist of two contributions.

$$\Delta G_{tot} = \Delta G_{bulk} + \Delta G_{surf} \quad (2)$$

with the Gibbs free energy of a bulk alloy given by[166]

$$\Delta G_{bulk} = X^{A}\Delta G_{l}^{A} + X^{Si}\Delta G_{l}^{Si} + RT(X^{A}\ln X^{A} + X^{Si}\ln X^{Si}) + G_{Exc}^{A\text{-}Si} \quad (3)$$

Here X^{Si} and X^{A} are the mole fractions of Si and the metal A, respectively, linked via the relation $X^{A} + X^{Si} = 1$. ΔG_{l}^{A} and ΔG_{l}^{Si} are the Gibbs free energies of the liquid phase relative to the solid phase of the respective element, RT is the product of the gas constant with the absolute temperature, and $G_{Exc}^{A\text{-}Si}$ is the excess Gibbs free energy of the liquid phase. The excess Gibbs free energy is customarily expanded as

$$G_{Exc}^{A\text{-}Si} = X^{A}X^{Si}\{L_{0}^{A\text{-}Si} + L_{1}^{A\text{-}Si}(X^{A} - X^{Si}) + L_{2}^{A\text{-}Si}(X^{A} - X^{Si})^{2} + L_{3}^{A\text{-}Si}(X^{A} - X^{Si})^{3}\} \quad (4)$$

with $L_{0}^{A\text{-}Si}$, $L_{1}^{A\text{-}Si}$, $L_{2}^{A\text{-}Si}$, and $L_{3}^{A\text{-}Si}$ being constants characteristic of the system in question. The surface contribution to the Gibbs free energy, again with respect to the solid phases of the elements, is given by

$$\Delta G_{surf} = \frac{2}{r}\{X^{A}(\sigma_{l}^{A}V_{l}^{A} - \sigma_{s}^{A}V_{s}^{A}) + X^{Si}(\sigma_{l}^{Si}V_{l}^{Si} - \sigma_{s}^{Si}V_{s}^{Si})\} \quad (5)$$

Here, σ_l (σ_s) and V_l (V_s) are the surface tension and molar volume of the liquid (solid) phase of the pure elements given.

Equation 5 is based on the simplifying assumptions that the surface tensions of liquid and solid can be directly inferred from the surface tensions of the pure elements, by assuming an ideal behavior and that the particle under consideration is a sphere of radius r.

At the eutectic temperature, the total Gibbs free energy as a function of X^{Si} exhibits a minimum, so that $\partial_{X^{Si}}\Delta G_{tot} = 0$. Since the total Gibbs free energy was taken relative to the solid phases of the respective elements, this minimum is located at $\Delta G_{tot} = 0$. Applying these two conditions to eqs 2−5, using $X^{A} = 1 - X^{Si}$, both eutectic temperature and composition can be directly calculated. The only things needed are temperature dependent expressions for the molar volumes, the surface tensions, the constants defining the excess Gibbs free energy, and the Gibbs free energies of the pure elements.

The Gibbs free energies of pure metals can be found in ref 167, and the parameters for the excess Gibbs free energy for Au, Ag, and Al are given by Tanaka et al.,[166] Chevalier,[168] and Jacobs,[169] respectively. The molar volumes of the liquid elements can be inferred from the data in the *CRC Handbook*,[170] and the molar volumes of the corresponding solids can be obtained by interpolating between the data at room temperature and at the melting point.[170,171] Surface tensions of liquid elements are listed by Keene,[172] and an estimate for the surface tensions of the solid elements is given by Tyson et al.[173]

Using these data, one can compute the radius dependence of the eutectic temperature shown in Figure 14. One can see that a decrease of the diameter leads to a decrease of the eutectic temperature and that the expected reduction of the eutectic temperatures is significant. Considering a 10 nm catalyst droplet, one can expect a shift of about 30 K for Au−Si and Al−Si and, even more pronounced, about 45 K for Ag−Si. One should, however, take into account that the accuracy of the data presented in 14 is limited by the fact that it is the difference between the surface tensions of liquid and solid that determines the magnitude of the effect and that, in particular, the data for the surface tension of the solid elements have to be considered as estimates. The overall accuracy of the data shown in Figure 14 is therefore probably not better than a factor of 2.

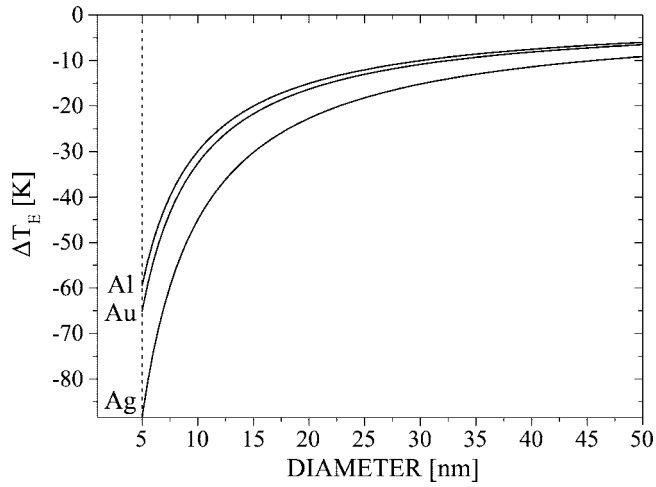


Figure 14. Shift ΔT_E of the eutectic temperature for the Au−Si, Al−Si, and Ag−Si systems as a function of the diameter.

7. Diameter Expansion of the Nanowire Base

This section is dedicated to the description of an interesting effect, namely the expansion of the nanowire diameter at its base, where it is attached to the substrate (see Figure 1c). The reason why it is presented here is that this diameter expansion nicely reflects the nature of the interaction between the liquid catalyst droplet and the nanowire. Yet, before coming to the diameter expansion itself, first some brief remarks on the concept of line tension.

As pointed out by Gibbs,[174] a line tension τ should in principle be assigned to dividing lines between different phases, in a completely analogously manner to assigning a surface tension to the dividing surface separating two phases. Contact lines occur in places where three phases meet. In our case, this concerns the triple-phase line, where vapor, droplet, and nanowire are in contact. Including such a line tension τ would, for instance, give an additional τ/r term to the equilibrium conditions defining the shape of the catalyst droplet, with r being the radius of the contact line. This is mentioned here because one can directly infer from this expression that the question of whether the line tension has to be considered or not largely depends on the size of the system in question. For macroscopic problems, the line tension can be omitted. The value of the line tension is usually estimated to be in the range 1×10^{-11} J m^{-1} to 1×10^{-9} J m^{-1}.[175] Such an order of magnitude can be expected from estimating that the line tension contribution to the energy of a single atom should be not much larger than the surface tension contribution. Surface tensions are typically on the order of 1 J m^{-2}, which together with an interatomic spacing of about 10^{-9} m corresponds to a line tension of not more than about 1×10^{-9} J m^{-1}. On the other hand, this estimate shows that, unless the radius r is just a few nanometers, the line tension can safely be neglected. This is also what we will do in the following discussion.

The diameters of Si wires or nanowires grown epitaxially on Si substrates typically show a diameter expansion at their base where they are attached to the substrate; see Figures 1c and 15.[16,18,176,177] At first glance, one might be tempted to assume that this diameter expansion is simply caused by an overgrowth of Si directly from the gas phase. A closer inspection, however, shows that there are mainly two arguments that speak against such a hypothesis. The first, put forward by Givargizov,[178] is that the observed diameter expansion at the wire base does not depend on the applied growth temperature to such an extent as one would expect if it were due to Si deposited from the gas phase. The second argument is that the shape of the expansion approximately scales with the diameter of the wire. Givargizov concluded that the "conical expansion at the whisker root must not be mistaken with an expansion due to overgrowth"[178] and that it "is evidently related to a change of the contact angle configuration".[178]

The fact that some change of the contact angle must occur in the initial phase of growth becomes apparent if the typical shapes of droplets on flat Si substrates are compared to those on top of Si wires. Au−Si alloy droplets on flat Si substrates and at temperatures of 400−650 °C show a contact angle (defined here as the angle within in the liquid) of about $\beta_0 \approx 43°$.[179] Au−Si droplets on top of wires are much more spherical, typically exhibiting contact angles of 90−120°.[36] It is evident that the droplet has to undergo some sort of transition in the initial phase of growth, and it is this change of the droplet shape that causes the observed expansion of

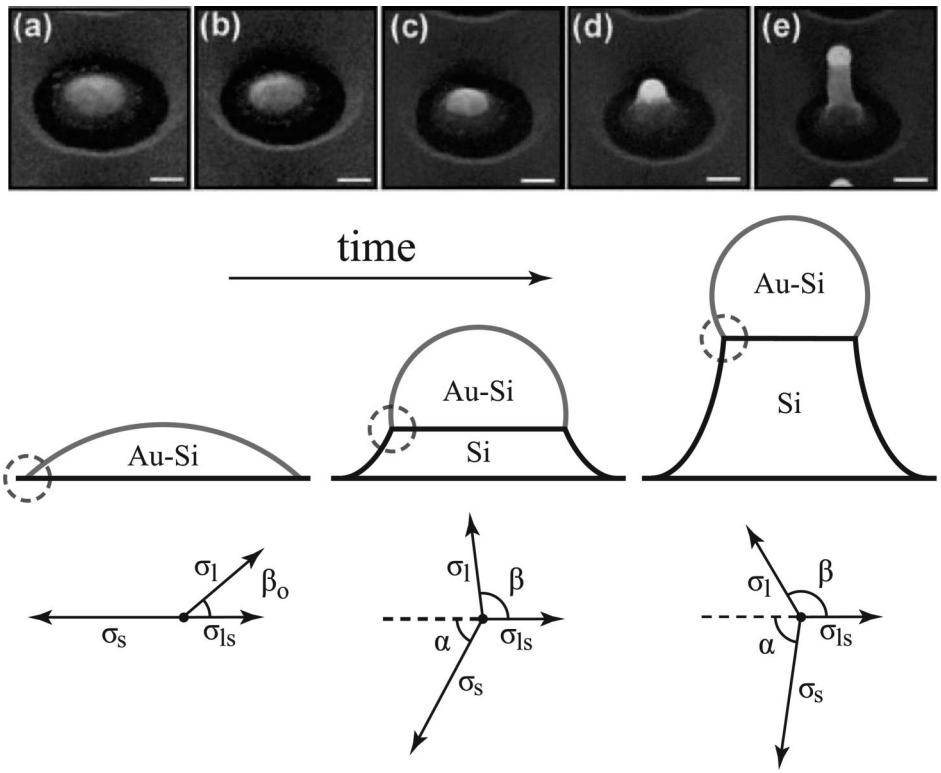


Figure 15. Top: Scanning electron micrographs indicating the development of the droplet shape in the initial phase of growth. Reprinted with permission from ref 29. Copyright 2008 American Institute of Physics. Center: Schematic development of droplet and wire shape in the initial phase of growth.[4,182] Bottom: the corresponding equilibrium balance of surface forces at the left edge of the droplet (dashed circles). Note: horizontal force components add up to zero.

the wire base. Several attempts have been made in the past to qualitatively describe this phenomenon.[176,180−182] We will follow here the work of Schmidt et al.[182] Please note that this model cannot be applied to templated nanowire growth and that it does not include any effects related to a surface faceting of the wires.

The three quantities necessary to describe the contact angle configuration of the droplet are σ_l, the surface tension of the liquid droplet, σ_s, the surface tension of the solid Si wire, and σ_{ls}, the interface tension liquid−solid interface. For brevity, σ_{ls} will in the following be referred to as a surface tension, though interface tension would be more precise. Suppose the wire growth velocity is small compared to the velocity with which the droplet reacts to changes of the boundary conditions. Then the development of the droplet−wire system can be described by a quasi-static growth model. This means that the development of the droplet−wire system with time corresponds to a sequence of equilibrium states. At equilibrium, the Neumann triangle relation[183,184] relates the contact angle β of the droplet to the inclination angle α of the nanowire flank and the surface tension values σ_s, σ_l, and σ_{ls}.

$$\sigma_l \cos(\beta) = \sigma_s \cos(\alpha) - \sigma_{ls} \tag{6}$$

In the case $\alpha = 0$, which corresponds to the case of a droplet on a flat substrate, eq 6 reduces to Young's equation. Equation 6 simply states that at equilibrium the horizontal components of the surface forces have to cancel out, so that there is no net force acting on the perimeter of the droplet. This is indicated in the bottom row of Figure 15, where the balancing of surface forces is depicted. When the shape of the droplet is approximated as a segment of a sphere, then the radius r of the liquid−solid interface can be expressed as a function of the contact angle β and the volume V of the droplet

$$r = \left(\frac{3V}{\pi}\right)^{1/3} \frac{(1 + \cos(\beta))^{1/2}}{(1 - \cos(\beta))^{1/6}(2 + \cos(\beta))^{1/3}} \tag{7}$$

The volume V of the catalyst droplet is taken to be constant during growth. The volume can also be expressed in terms of the initial radius r_0 of the liquid−solid interface and the initial contact angle β_0; initial here means prior to growth, that is at $\alpha = 0$.

$$V = \frac{\pi}{3}\left(\frac{r_0}{\sin(\beta_0)}\right)^3 (1 - \cos(\beta_0))^2(2 + \cos(\beta_0)) \tag{8}$$

The angle α, the inclination angle of the wire flanks, can be trivially related to the slope of the wire flank:

$$\frac{dh(r)}{dr} = -\tan(\alpha) \tag{9}$$

with h being the height of the wire. This differential equation can now be solved for h by a simple numerical integration, done most easily using $\cos(\alpha)$ as integration variable. This then gives the shape of the wire expansion for a certain configuration of surface tensions. For Au-catalyzed VLS Si wire growth, the surface tension of the liquid droplet $\sigma_l \approx 0.85$ J m^{-2},[185] the surface tension of Si $\sigma_s \approx 1.24$ J m^{-2},[186] and the initial contact angle $\beta_0 \approx 43°$[179] can be used to deduce the liquid−solid interface tension $\sigma_{ls} \approx 0.62$ J m^{-2}. The shape at three different stages of growth is schematically shown in the middle row of Figure 15. A comparison of calculated with experimentally observed shapes can be found in the work of Schmidt et al.[182]

To summarize, wires grown on a substrate usually show a diameter expansion at their base, which is caused by a change of the droplet shape. Considering the equilibrium balance of surface tensions and the corresponding droplet shape, a model for the expansion at the wire can be derived that qualitatively describes the experimentally observed phenomenon.

8. Surface Tension Criterion

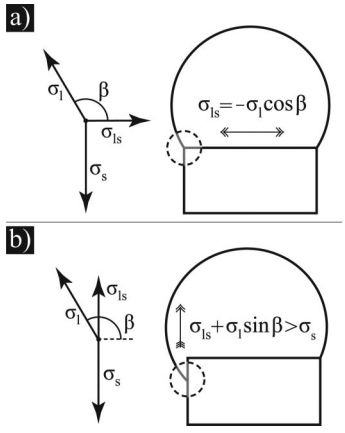
As already mentioned in subsection 3.2.2, growth of Si wires using type-B catalysts such as In or Ga does require harsher growth conditions than Au-catalyzed growth. This might be caused by the low Si solubility at the respective growth temperature, as a correlation between Si solubility and growth velocity has been demonstrated.[11] An alternative explanation could be that the surface tension of these type-B catalysts is simply too small. According to Nebolsin et al.,[93] a certain minimum value for σ_l, the surface tension of the droplet, is required for stable VLS wire growth. This will now be laid out in detail.

Let us first consider the situation shown in Figure 16a. Suppose the droplet can freely adjust its perimeter during growth, then the horizontal components of surface forces need to cancel out, as already discussed in the previous section. Growth at constant radius means that

$$\sigma_l \cos(\beta) = -\sigma_{ls} \tag{10}$$

One can see that eq 10 is equivalent to the equilibrium condition of eq 6, with $\alpha = 90°$.

Now, let us assume that, by some fluctuation or perturbation, a situation occurs where the droplet wets the side surface of the wire, as depicted in Figure 16b. For the position of the droplet, as shown in Figure 16a, to be stable and not only metastable, there must be a vertical net force acting on the part of the droplet wetting the nanowires side in Figure 16b, so that the droplet can recover its original position, once it lost its foothold. According to the force balance scheme shown in Figure 16b, such a vertical force on the triple phase line of the droplet exists if the following inequality holds:



c)

	σ_l [Jm^{-2}]	T [K]	%Si
Ni	1.30	1266	59
Pd	1.24	1165	52
Cu	1.23	1076	31
Au	1.22	636	19
Pt	1.22	1252	67
Ag	0.92	1108	11
Al	0.89	850	12
Zn	0.79	693	0
Ga	0.69	700	0
In	0.53	700	0
Bi	0.37	700	0

Figure 16. (a) Equilibrium shape of the droplet during growth; the horizontal force compontents have to cancel out. (b) Nonequilibrium situtation after some perturbation; a net vertical force is required to reestablish equilibrium. (c) Surface tension of different metal−Si alloy catalyst systems, after Keene,[172] calculated at the temperatures and compositions given in the two neighboring columns.

$$\sigma_l \sin(\beta) + \sigma_{ls} > \sigma_s \tag{11}$$

By combining eqs 10 and 11, one can arrive at the following inequality that must be fulfilled for stable Si nanowire growth.

$$\sigma_l > \sigma_s/(\sin(\beta) - \cos(\beta)) \tag{12}$$

Now, $\sin(\beta) - \cos(\beta)$ is always smaller than $\sqrt{2}$, so the rhs of eq 12 is always greater than $\sigma_s/\sqrt{2}$. Consequently, stable wire growth cannot be realized when

$$\sigma_l < \sigma_s/\sqrt{2} \tag{13}$$

This is the surface tension criterion first derived by Nebolsin et al.[93] Assuming a Si surface tension σ_s of about 1 J m^{-2}, eq 13 leads to a threshold for σ_l of about 0.7 J m^{-2}. If the surface tension σ_l of the liquid droplet is smaller than about 0.7 J m^{-2}, then, according to this model, the droplet should not be dewet from the sides of the wire, if by some perturbation the droplet did wet them before. Growth is then said to be unstable.

This surface tension criterion proves to be particularly insightful if applied to the different VLS catalyst materials. In Figure 16c, the surface tensions for the different catalysts are listed, which were calculated by using the surface tension values of the pure elements given by Keene[172] and by assuming that the surface tension σ_l of the metal−Si catalyst droplet is equal to $(1 - X^{Si})\sigma_l^{metal} + X^{Si}\sigma_l^{Si}$, with X^{Si} being the Si concentration in the droplet. As a temperature, we chose the smallest possible temperature at which VLS growth may take place. The corresponding composition at this temperature was obtained from the respective binary phase diagram.[123] In the case of Ga, In, and Bi, a temperature of 700 K was chosen instead of the eutectic temperature, simply because the eutectic temperatures are so low that it seems unrealistic that Si wires can actually be grown at these temperatures.

In Figure 16c one can see that metal−Si catalyst droplets of the type-C metals Ni, Pd, Cu, and Pt would have surface tensions that would well fulfill the stability criterion. This seems to be consistent with the observations that VLS growth using these metals gives good results.[7,16,93] This is also true for Au. Metal−Si catalyst droplets of the other two type-A metals, Ag and Al, have a lower surface tension, and according to Nebolsin et al.,[93] the growth stability using Al is already lower than that of Au. But still, the stability criterion should be fulfilled. The type-B metal Zn, on the hand, is already closer at the limit. Nebolsin et al.[93] state that the stability of Zn-catalyzed growth is low. Among the type-B metals, Zn has the highest surface tension, which fits to the experimental observation that, among the type-B metals, Zn seems to work best.

The surface tensions of Ga and In are even lower, probably lower than the threshold $\sigma_l/\sqrt{2}$, but not very much. Growth with Ga[37,39,93,99,107] and In[40,93,100,107,108] is possible but only by applying rather harsh growth conditions. This is also true for Si nanowire growth using Bi,[57] despite its low surface tension of about 0.4 J m^{-2}.

In conclusion, the surface tension of the catalyst droplet should have an effect on the stability of the droplet−nanowire system. However, as Bi-catalyzed growth shows, the stability criterion cannot be deemed as an exclusive criterion for the possibility of growing nanowires. Nevertheless, the overall trend that Si nanowire growth becomes more difficult the smaller the surface tension of the droplet is seems to be valid.

9. Growth Velocity and Gibbs−Thomson Effect

The focus of this section is on the diameter dependence of the nanowire growth velocity induced by the Gibbs−Thomson effect. The Gibbs−Thomson effect can be most easily understood by considering the energetics of a small spherical droplet or particle. The chemical potential μ is the energetic price per atom one has to pay for adding another atom of the same species to the system. For small systems having high surface-to-volume ratios, the influence of the surface on the thermodynamics cannot be neglected. It is evident that increasing the number of atoms N must necessarily be accompanied by an increase of the surface area and that one has to pay the energetic price for that surface increase as well. For a spherical droplet of radius R and volume $4\pi/3R^3 = N\Omega$, with Ω being the volume per atom (assumed to be constant here), the Gibbs free energy G can be expressed as $G = \mu_\infty N + 4\pi R^2\sigma$, with σ being the surface free energy and μ_∞ being the bulk (infinite radius) chemical potential. By using $\partial R/\partial N = \Omega/(4\pi R^2)$, one can easily derive that the chemical potential $\mu = \partial G/\partial N$ is given by $\mu = \mu_\infty + 2\Omega\sigma/R$. This radius dependence of the chemical potential is usually referred to as the Gibbs−Thomson effect.

For a cylindrical wire, things are very much the same, but one has to be careful with the quantities that are kept constant and those that are not. The Gibbs free energy of a wire of length L, radius r, and surface free energy σ is given by $G = \mu_\infty N + 2\pi r^2\sigma + 2\pi rL\sigma$. Suppose the wire only changes in length; that is, taking the radius to be constant and using $\partial L/\partial N = \Omega/(\pi r^2)$ the chemical potential $\mu = (\partial G/\partial N)_r$ becomes[178]

$$\mu = \mu_\infty + \frac{2\Omega\sigma}{r} \tag{14}$$

Thus, we arrived at the same expression as for a sphere. The interesting feature about this expression, however, is the factor of 2 in the numerator. This factor occurs because the radius was taken to be constant. One can easily derive that this factor of 2 is absent in the case of a wire that can expand in radius but not in length. This derivation is presented here just because there seems to be some confusion in the literature concerning this factor of 2 in the Gibbs−Thomson formula for nanowires.

The radius dependence of the chemical potential, as implied by the Gibbs−Thomson effect, causes the growth velocity to become diameter-dependent, as observed by several groups.[10−12,112,144,187,188] What is interesting about this diameter dependence of the growth velocity is that the problem is coupled to the question of what the rate determining step of VLS wire growth is. Givargizov divided the growth process into three main steps.[10] In the first step, Si precursor molecules are cracked at the surface of the catalyst droplet and Si is incorporated into the droplet. This step will be referred to as the incorporation step in the following, and the rate [atoms/s] by which it proceeds will be called the incorporation rate. After the incorporation of Si, Si diffuses through the droplet surface to the nanowire−droplet interface. This is the diffusion step. In the last step of the process, Si crystallizes at the liquid−solid interface and forms the Si nanowire. This will be referred to as the crystallization step, proceeding at a rate [atoms/s] called the crystallization rate.

Givargizov neglected the diffusion step, arguing that diffusion through a microscopic droplet is simply too fast to seriously affect the growth velocity.[178] Regarding the other two steps of the growth process, the incorporation step and the crystallization step, there was some discussion regarding which step determines the wire growth velocity. Bootsma and Gassen[30] argued that the growth velocity evidently depends on the precursor pressure and concluded from this observation that incorporation must be the rate determining step. Givargizov, on the other hand, argued in favor of the crystallization rate;[178] his argument for the crystallization step as the rate determining step was mainly based on the observation that the growth velocity does depend on the crystallographic orientation of the wires. Both arguments are valid, and there seems to be a dilemma here. This dilemma, however, can be solved by disregarding the assumption of a single rate determining step. Assuming instead that it is not a single step that determines the growth rate but rather the interplay between both steps allows us to reconcile the arguments.

The key parameter for the wire growth velocity is the Si supersaturation, defined as the difference between the chemical potential of Si dissolved in the catalyst droplet and the Si chemical potential of the nanowire. A certain supersaturation is required for the nucleation of Si at the liquid−solid interface. Hence, the crystallization rate can be expected to be a function of the supersaturation and to increase with increasing supersaturation. Let us for now assume that also the incorporation rate depends on the supersaturation. The reason is that an increase of the supersaturation also reduces the chemical potential difference between Si in the vapor and Si in the droplet, which could in turn potentially reduce Si incorporation. Accordingly, the incorporation rate can be expected to decrease with increasing supersaturation. The case where it is independent of the supersaturation can then still be derived.

What must be clear, however, is that, under steady state growth conditions, the incorporation rate has to equal the crystallization rate. This condition demanding equal rates then couples the incorporation rate to the crystallization rate; and since both depend on supersaturation, the supersaturation at steady state will adjust at a level where both rates are equal. The level at which the steady state supersaturation $\Delta\mu$ finally settles depends on the supersaturation dependence of both the incorporation and the crystallization rate.

In order to keep formulas short, it is useful to transform the rates [atoms/s] into velocities [m/s] by multiplying them with $\Omega/(\pi r^2)$. As already mentioned, at steady state, incorporation and crystallization velocity necessarily have to be equal. Imagining a velocity vs supersaturation plot, this equality means that the steady state situation is defined by the crossing point of the two velocity curves. The y-axis position of this crossing point then defines the steady state growth velocity v, and the x-axis position of the crossing point defines the steady state supersaturation $\Delta\mu$. The derivatives of the incorporation and crystallization velocity with respect to the supersaturation, computed at this crossing point, shall be called α and ω, respectively. These derivatives can then be used in a Taylor expansion to first order, by means of which one arrives at a general expression for the radius dependence of the steady state supersaturation (for more details, see ref 189).

$$\Delta\mu = \Delta\mu_\infty + \frac{\alpha_1}{\omega_1 - \alpha_1}\frac{2\Omega\sigma_s}{r} \tag{15}$$

The steady state growth velocity becomes

$$v = v_\infty + \frac{\omega_1 \alpha_1}{\omega_1 - \alpha_1} \frac{2\Omega\sigma_s}{r} \quad (16)$$

Here $\Delta\mu_\infty$ and v_∞ are the steady state supersaturation and the steady state growth velocity at infinite radius, Ω is the volume per atom, and σ_s is the surface free energy of silicon, respectively. In this linear approximation, both $\Delta\mu$ and v show a $1/r$ dependence that is proportional to an undetermined prefactor; and this prefactor depends on the slopes α and ω of the incorporation and crystallization velocities. As discussed above, one usually expects α to be negative and ω to be positive. Thus, both prefactors in eqs 15 and 16 become negative and $\Delta\mu$ and v are therefore expected to decrease with decreasing radius.

In Figure 17 the growth velocity data of Schmid et al.[188] are plotted as a function of the inverse nanowire radius. One can see that the data reasonably well agree with a linear dependence on inverse radius with negative slope, which is what was expected. It should, however, be noted here that a nicely linear behavior is not always observed. There are cases where the first order calculation does not provide a satisfyingly accurate description of the radius dependence of the growth velocity (see refs 10, 11, and 112). Givargizov, for instance, fitted his growth velocity data with the function $v = (c_1 + c_2/r)^2$, with c_1 and c_2 being constants.[10] Such a fit function, however, means nothing more than that a $1/r^2$ term also contributes to the diameter dependence of the growth velocity; and such a term can be derived by including higher order terms in the Taylor expansion.

The general expression (eq 15) can now be used to derive the special case where the crystallization step is indeed rate-determining. By taking the limit ($\alpha \rightarrow \infty$), this leads to

$$\Delta\mu = \mu_\infty - \frac{2\Omega\sigma_s}{r} \quad (17)$$

This expression is consistent with the result derived by Givargizov for the case that crystallization alone determines the wire growth rate.[10] The aforementioned case of an incorporation velocity that does not depend on supersaturation can also be derived from the general expressions. Taking the limit ($\alpha \rightarrow 0$) of eq 16, one can see that the radius dependence vanishes, which is in accordance with what has been reported by Kodambaka et al.[36]

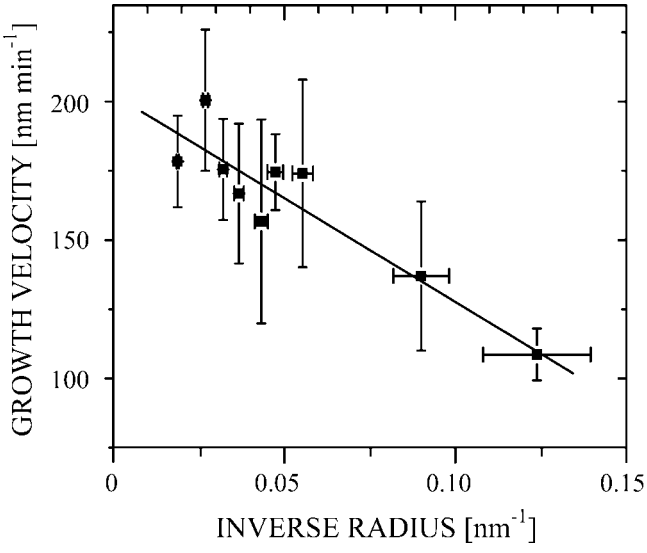


Figure 17. Nanowire growth velocity as a function of the inverse nanowire radius using the data of Schmid et al.;[188] after Schmidt et al.[4]

As shown in Figure 17, the nanowire growth velocity can be expected to decrease with decreasing radius, because of the increase of the Si chemical potential of the wire due to the Gibbs−Thomson effect. Growing thin nanowires is simply accompanied by the creation of a lot of surface area per Si volume. One can easily understand that one direct consequence of the above-described radius dependence is that for a given temperature and pressure a critical minimum radius should exist for which the growth velocity becomes zero. Zero growth velocity should occur when $\Delta\mu$ becomes zero, or at least the growth velocity should be so small as to prevent further Si crystallization. This idea of a critical radius at which the growth velocity becomes zero was first mentioned by Wagner and Ellis.[16] A thorough treatment of this matter was published by Tan et al.[190,191]

A very interesting experimental study on this subject was published recently by Dhalluin et al.[192] The authors employed the fact that the side faces of Si nanowires are often seen to be decorated with tiny Au islands,[24,43,62] and they used these tiny gold islands to study the pressure dependence of the critical radius. For this, after growing Si nanowires under usual conditions, they increased the silane pressure sharply until very tiny nanowires, catalyzed by these nanometer-sized Au islands decorating the surface, commenced growing.[192] The authors then determined the critical radius as a function of applied pressure. Their observed pressure dependence is in full accordance with a radius dependence of the supersaturation as given by eq 17. In fact, one can use their data to obtain an estimate for the silicon surface tension.[4]

10. Doping

For bulk Si, it is easy to determine the dopant concentration. One can simply measure the resistivity (e.g., by four probe measurements) and use existing calibration curves[193] to relate the resistivity to the impurity concentration. Considering Si nanowires, however, applying bulk Si calibration curves may lead to wrong doping concentration values. This can be inferred from the work of Wang et al.,[42] who determined the resistivity of phosphorus doped Si nanowires from four probe measurements and the corresponding actual dopant concentration, N_D^0, using secondary ion mass spectroscopy (SIMS). Comparing these results to the bulk Si resistivity-vs-*P*-concentration calibration curves, one finds that the resistivity of the nanowires is about 1 to 2 orders of magnitude higher than what one would naively expect. Expressed differently, if the authors would have only measured resistivity and used the bulk Si calibration curve for *P* to deduce the dopant concentration, they would have underestimated the *P* concentration by about a factor 10−100. Even at diameters greater 10 nm, that is, at a size where quantum confinement effects can still be neglected,[192] nanowires may behave differently than bulk material. This and the subsequent sections focus on the main effects responsible for the difference in electrical characteristics between nanowires and bulk Si.

Considering p-type bulk Si, the conductivity is proportional to the hole density, p, and the hole mobility, μ_p. Concerning the charge carrier density, one usually assumes that the hole concentration p is basically equal to the total concentration of acceptor dopant atoms, N_A^0 (subscript A for acceptor). Yet, one has to be careful here, because setting N_A^0 equal to p implies that three separate assumptions must be fulfilled. The

first assumption is that the total acceptor concentration, N_A^0, equals the concentration of potentially ionizable acceptors, N_A, that is, that all dopant atoms are properly substitutionally incorporated into the Si crystal (often they are then said to be activated). Second, one implicitly assumes that these activated acceptors are also fully ionized, i.e. $N_A = N_A^-$, with N_A^- being the concentration of ionized acceptors. The third implicit assumption is that $N_A^- = p$, i.e. that the hole concentration can be approximated to be equal to the density of ionized acceptors. In this section, but mainly in sections 11 and 12 following thereafter, a closer look is taken into the validity of these three approximations.

Semiconductor functionality crucially depends on the possibility of adjusting the electronic properties by the addition of dopants. Dopants are shallow level impurities such as B, P, As, Ga, Al, or Sb (see Figure 11) that can act as donors or acceptors of charge carriers. In order to become electrically active, the dopant atoms need to be substitutionally incorporated into the silicon lattice.[194] So one has to be precise about what is meant by dopant concentration. On the one hand, there is the total donor (acceptor) concentration N_D^0 (N_A^0), which is what one would obtain by simply counting the number of dopant atoms found in a certain volume, e.g. using secondary ion mass spectroscopy (SIMS). Yet, the thus obtained dopant concentrations, N_D^0 (N_A^0), do not necessarily agree with the density of electrically active donors (acceptors), N_D (N_A). One possible cause for such a disagreement could be that dopant atoms, though being present, are not properly substitutionally incorporated; a scenario that for instance occurs when dopant atoms are implanted into Si. After dopant implantation, an additional thermal treatment is required to activate the dopants. Another possibility is that dopant atoms are located at the nanowire surface, which would also render them electronically inactive. Although these dopants would be counted by SIMS measurements, they would not affect the electronic properties. At least for very thin Si nanowires, calculations showed that there indeed exists a certain tendency of B or P atoms to diffuse to the surface.[195]

There are different ways to dope Si nanowires, with one being the use of a catalyst metal such as In,[40,108] Ga,[37,39,99] or Al that by itself would cause a doping.[40,95,96,99] Although there are good reasons to believe that the resulting wires would indeed be highly p-doped, direct evidence for the effectiveness of such an approach still seems to be missing. Alternatively, one could also add a small amount of a dopant metal to a catalyst such as Au, in the hope that some dopant atoms will be released and incorporated into the nanowires during growth. The feasibility of such an approach has been demonstrated, though the method seems to be not very effective.[196]

An approach that in principle offers much better controllability of dopant type and density is to directly supply the dopant during growth. This can be done either by a coevaporation or coablation of Si and dopant in the case of MBE nanowire growth[65] or laser ablation,[80,197,198] respectively, or by supplying both Si and dopants in the form of gaseous precursors in the case of CVD nanowire growth.[199,200] The latter appears to be the most promising approach, and we will concentrate on gas phase doping in the following.

In Figure 18, a collection of resistivity data is shown as a function of the silane to dopant precursor ratio data, considering different precursors such as phosphine (PH_3), diborane (B_2H_6), and trimethylborane (TMB), ($B(CH_3)_3$). The

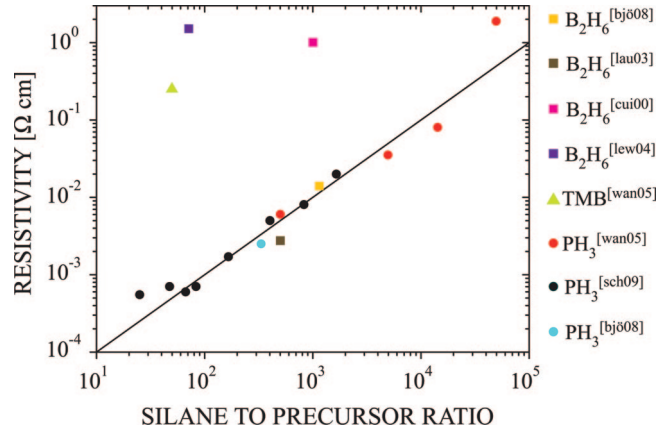


Figure 18. Si nanowire resistivity as a function of the silane to dopant precursor ratio using data of [bjö08],[236] [lau02],[157] [cui00],[81] [lew0],[201] [wan05],[42] and [sch09].[188] The straight line has unit slope. After Schmidt et al.[4]

phosphine data in Figure 18 indicate that the resistivity can indeed be varied over orders of magnitude by changing the silane/phosphine ratio. They furthermore show that the resistivity is approximately inversely proportional to the PH_3/SiH_4 ratio, with the black line in Figure 18 having unit slope. Concerning possible effects of phosphine on the nanowire growth, it has been reported that phosphine does not induce a tapering of the nanowires and that the nanowire growth rate is almost unaffected.[188] Phosphine, therefore, seems to be the precursor of choice for obtaining n-type Si wires. There is only one complication related to the use of phosphine, namely that nanowire yield is reduced for very high phosphine-to-silane ratios, up to a point where nucleation is completely inhibited, occurring at phosphine-to-silane ratios greater than 0.02.[188] Similar results have previously been reported for the use of arsine.[29] Arsine is known to affect the growth of Si wires,[10,28] presumably by changing their surface tensions.

The data on the use of diborane as p-type dopant precursor are far less consistent. To some extent, this inconsistency is probably caused by the fact that the addition of diborane facilitates the growth of an amorphous Si shell.[201] Since the resistivity of amorphous Si is higher than the resistivity of crystalline Si, the presence of an amorphous shell could explain the relatively large resistivity values reported by Lew et al.[201] and Cui et al.[81] Considering silane CVD processes, a possible strategy to suppress the diborane-induced deposition of Si on the wire surface is to increase the hydrogen pressure, as it is known that the addition of hydrogen reduces the Si deposition rate.[202,203] Another possible approach to avoid an unintended side deposition is to use trimethylboron, TMB, instead of diborane, as demonstrated by Lew et al.[201] SIMS measurements performed on these wires, however, indicated that the B incorporation efficiency is about 2 orders of magnitude smaller for TMB,[42] and hence, higher TMB pressures therefore need to be applied.

11. Dopant Ionization

Considering bulk Si measurements at room temperature, one usually assumes that the dopant atoms are fully ionized, so that the concentration of ionized donors N_D^+, for example, can be taken to be equal to the concentration of electrically active donors N_D. Yet, one has to be careful in applying such an assumption to Si nanowires, because the ionization energy, i.e. the energy difference between the donor (acceptor) level

and the conduction (valence) band, depends on the electrostatics of the surrounding material. The reason why only little energy is needed to ionize dopants is that the electrostatic potential of the ionized impurity is shielded by charge carriers in Si. Thus, when the volume of Si surrounding the dopant atom is reduced, also the shielding of the electrostatic potential is reduced, which in turn causes an increase of the ionization energy. For Si nanowires, this means that the dopant ionization efficiency should depend on the nanowire radius; and since it is an electrostatic problem, one can expect that the ionization efficiency also depends on the dielectric constant of the medium surrounding the nanowire.

Diarra et al.[204] investigated the diameter dependence of the ionization energy of dopants in semiconducting nanowires caused by the dielectric confinement. They found that the radius dependence of the ionization energy $E_I(r)$ of a dopant is given by

$$E_I(r) = E_I^0 + \frac{2}{r\varepsilon_{nw}}\frac{\varepsilon_{nw} - \varepsilon_{out}}{\varepsilon_{nw} - \varepsilon_{out}}F\left(\frac{\varepsilon_{nw}}{\varepsilon_{out}}\right) \quad (18)$$

with E_I^0 being the ionization energy of the dopant in bulk Si, and r the nanowire radius. ε_{nw} and ε_{out} denote the relative permittivity of the nanowire and the medium surrounding the nanowire, respectively. According to Niquet et al.,[205] the function $F(x)$ can be approximated as

$$F(x) = \frac{200.674 + 175.739x + 17.395x^2 + 0.0949x^3}{219.091 + 50.841x + x^2} \quad \text{eV nm} \quad (19)$$

Considering the ionization energy of a Si nanowire ($\varepsilon_{nw} = 11.7$) in vacuum or air ($\varepsilon_{out} = 1$), one arrives at the following expression for the radius dependence of the ionization energy

$$E_I(r) = E_I^0 + \frac{0.7255\ \text{eV nm}}{r} \quad (20)$$

Thus, the ionization energy acquires a significant radius dependence, being quite pronounced for small radii. One should, however, add here that the expressions by Diarra et al.[204] are only valid as long as quantum effects can be neglected, which restricts the applicability to Si nanowires with diameters greater than approximately 10 nm.[192]

Such a change of the ionization energy must, of course, be accompanied by a change of the ionization efficiency, which is defined as the density of ionized dopants divided by the total density of dopants. If only one type of dopant is present and if doping is not too low such that the contribution of the minority charge carriers does not alter the charge balance significantly, the concentration of ionized donors N_D^+ or acceptors N_A^- is approximately given by[193,206]

$$N_D^+ = \frac{N_c}{4}e^{-E_I/kT}\left(-1 + \sqrt{1 + 8\frac{N_D}{N_c}e^{E_I/kT}}\right) \quad (21)$$

$$N_A^- = \frac{N_v}{8}e^{-E_I/kT}\left(-1 + \sqrt{1 + 16\frac{N_A}{N_v}e^{E_I/kT}}\right) \quad (22)$$

N_c and N_v are the density of states in the current and valence band, respectively. One can easily see from eq 21 that ionization efficiency depends on the doping level. To illustrate this effect, the ionization efficiency of P in Si is shown in Figure 19 as a function of the nanowire diameter, considering various different donor concentrations N_D. It is apparent that, especially for thin Si nanowires with diameters of 15 nm or less and moderate doping, the effect of the dielectric confinement on the ionization efficiency is quite pronounced. For Si nanowires of this size, a reduction of the ionization efficiency can be expected to have a major influence on the electric characteristics of the nanowires.[207] Therefore, the dielectric confinement has to be taken into account when thin nanowires are considered.

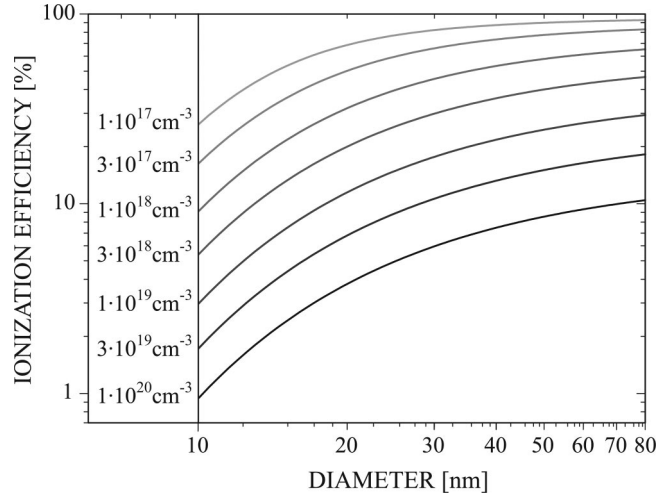


Figure 19. Ionization efficiency of phosphorus impurities ($E_I^0 = 45$ meV[204]) as a function of the nanowire diameter given for various donor concentrations N_D using the expression of Diarra et al.[204] Temperature is 300 K.

12. Surface States and Charge Carriers

One of the main reasons why Si is the material of choice for electronics applications is that Si possesses a chemically stable oxide, SiO_2, which can furthermore also well passivate the Si surface. For Si based electronic devices such as, for example, field-effect transistors (FETs), a good isolation oxide with a low level of charge stored in the oxide or at the Si−oxide interface is of utmost importance. The quality of the oxide and Si−oxide interface of course does not only matter for traditional top-down Si devices but also for Si nanowires. Especially for thin Si nanowires with large surface-to-volume ratios, surface properties may have significant influence on the electrical characteristics. To quantify the influence of the surface states on the electrical properties of Si nanowires will be the focus of this section.

Following the nomenclature of Deal,[208] one distinguishes between four different categories of charges that may occur in or at the Si−SiO_2 interface. The first two categories regard charges that are located deep inside the oxide. Charges can be either oxide trapped charges (density Q_{ot}) or mobile ionic charges (density Q_m). Charges at or in close vicinity to the Si−SiO_2 interface can either be fixed oxide charges (density Q_f) or—and this is what this section is about—interface trapped charges (density Q_{it}). The main difference between the fixed oxide charges and the interface trap charges is that the fixed oxide charges do not depend on the position of the Fermi level in the underlying Si. The main effect of Q_{ot}, Q_m, and Q_f is to change the electrostatic boundary conditions. Considering field effect transistor characteristics, their effect would correspond to an additional gate bias.

More interesting and presumably also more important for the electrical properties are the interface trap charges (density Q_{it}). Their charge density does depend on the position of the Fermi level, as they can exchange charges with Si. The

interface trap charge density Q_{it} is caused by states at the $Si-SiO_2$ interface that can either trap or release single electrons, depending on the position of the Fermi level. The density of these trap states varies within the Si band gap, and they are therefore characterized by the interface trap level density D_{it} [eV^{-1} cm^{-2}]. The interface trap level density D_{it} of a $Si-SiO_2$ interface is U-shaped as a function of energy, with the minimum located at the band gap middle.[193,209] Concerning the physical nature of these trap states, it was found that the presence of such interface trap states can be related to the presence of so-called P_b resonance centers, observed in electron spin resonance experiments.[210−212] It could also be shown that these P_b centers are indeed the main source for the interface trap states.[213−219] Furthermore, it was found that the P_b centers correspond to trivalent Si atoms bonded to just three other Si atoms.[214,220] In a crude approximation, one could say that the interface trap states are nothing more than Si dangling bonds; and thinking of interface states as dangling Si bonds, it is also intuitively understandable that they can act as both donors and acceptors. The states below the middle of the band gap are donor like, which means they are either neutral or positively charged. The states in the upper half of the band gap are acceptor like, for example, they are either neutral or negatively charged. Whether these states are charged or not depends on the position of the Fermi level at the Si surface. Considering an n-type Si wire with the Fermi level located in the upper half of the band gap, all interface trap states between the Fermi level and the band gap middle trap one electron each and become negatively charged. The necessary electrons have to be taken from the underlying Si, causing the n-type Si near the surface to acquire a net charge, which in turn causes a band bending; see Figure 20a. Schmidt et al.[221] investigated such a scenario, adopting the full depletion approximation and taking the dopants to be fully ionized. In view of the discussion in the previous section, it seems to be an oversimplification to assume that dopants are fully ionized. Their model, however, can be easily extended to also include the diameter dependence of the dopant ionization, if it is assumed that the ionization efficiency is not affected by the presence of interface states.

Let us consider an n-type Si nanowire of radius r_{nw}, with a density of ionized donors, N_D^+, according to eq 21. In the absence of interface traps, the position of the Fermi level ψ_0 [eV] at radius $r = 0$ expressed with respect to the band gap middle (see Figure 20a) is given by

$$\psi_0 = kT \ln\left[\frac{N_D^+ + \sqrt{(N_D^+)^2 + 4N_c N_v e^{-E_g/kT}}}{2N_c e^{-E_g/kT}}\right] \quad (23)$$

with N_c and N_v being the density of states in the conduction and valence bands, respectively, and E_g being the band gap width. To keep the calculation concise, one can introduce a parameter

$$\chi = q^2 N_D^+ r_{nw}^2/(4\varepsilon_{nw}\varepsilon_0) \quad (24)$$

with ε_0 being the vacuum permittivity and q being the elementary charge.

As mentioned above, surface states will cause a depletion of the Si in the vicinity of the surface by trapping charge carriers. In the full depletion approximation the semiconductor is divided into two regions (see Figure 20a): a surface-near region, that is fully depleted and a nondepleted region

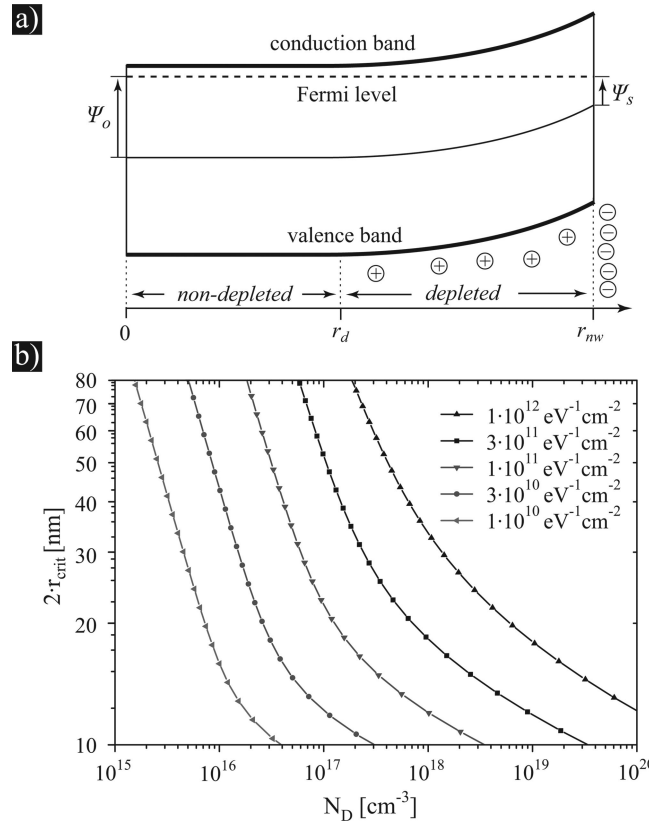


Figure 20. (a) Schematic band bending in an n-doped Si nanowire caused by surface traps in the full depletion-approximation. The nanowire is nondepleted between its center and the depletion radius r_d, and it is depleted from r_d to its surface at r_{nw}. ψ_o and ψ_s classify the position of the Fermi level with respect to the band gap middle at the nanowire center and the surface, respectively. (b) Critical diameter $2r_{crit}$ for different interface trap level densities D_{it} as a function of the donor concentration N_D; dopant is P with a bulk ionization energy of 45 meV; temperature is 300 K.

below. The boundary between these two regions is the depletion radius r_d, which is given by

$$r_d = r_{nw}\sqrt{1 - \left(\frac{2D_{it}\psi_0}{r_{nw}N_D^+ + 2\chi D_{it}}\right)} \quad (25)$$

The main factor that determines r_d is, of course, the interface trap level density D_{it}, the source for the depletion. In the case $0 < r_d < r_{nw}$, the nanowire is said to be partially depleted. It is said to be fully depleted if $r_d = 0$. The interesting question is at which point full depletion sets in. Suppose the values of D_{it} and N_D^+ are given; then full depletion occurs for nanowire radii that are smaller than the critical radius

$$r_{crit} = \frac{\varepsilon_{nw}\varepsilon_0}{q^2 D_{it}}\left(-1 + \sqrt{\frac{4q^2 D_{it}^2 \psi_0}{N_D^+ \varepsilon_{nw}\varepsilon_0}}\right) \quad (26)$$

This expression can be approximated as $r_{crit} \approx 2D_{it}\psi_0/N_D^+$. For applications where a full depletion of the nanowires is not desired, the question arises regarding what dopant concentrations are necessary to prevent a nanowire of a certain diameter from becoming fully depleted and how the minimally required doping changes with the density of interface traps or, equivalently, the quality of the Si/SiO_2 interface. This is shown in Figure 20b, where the critical diameter necessary to prevent a full depletion of the nanowire

is displayed as a function of the dopant concentration and for different interface trap level densities D_{it}.

One can see in Figure 20b that the critical diameter crucially depends on the D_{it} value. For Si nanowires with diameters as low as 10 nm, it is obviously essential to try to improve the Si−SiO_2 interface quality and reduce interface trap densities. A lowering of the interface trap level density can be achieved by a high temperature annealing in oxygen atmosphere, giving a high quality oxide, followed by a short annealing in hydrogen atmosphere that serves to passivate remaining interface states. In this way, the interface trap level density D_{it} can be reduced from about 1×10^{12} eV^{-1} cm^{-2} to values smaller than 1×10^{11} eV^{-1} cm^{-2}.[193] The density of surface charges of Si nanowires has been investigated by Seo et al.[222] and Kimukin et al.,[223] and they found a surface charge density of $(2-3) \times 10^{12}$ cm^{-2} in as-grown Si nanowires. As expected, Seo et al.[222] found that the surface charge density can be reduced by replacing the native oxide with a high quality thermal oxide.

Furthermore, one can see in Figure 20b that the curves in this log−log plot are basically linear for diameters larger than about 25 nm. The fact that they start to bend at smaller diameters and higher dopant concentrations is due to the reduced ionization efficiency, as shown in Figure 19.

In order to calculate the average charge carrier density for both partially and fully depleted nanowires, one has to solve the Poisson equation and calculate ψ_s [eV], the position of the Fermi level (defined here with respect to the band gap middle; see Figure 20a) at the nanowire surface.

$$\psi_s = \psi_0 - \chi \frac{(r_{nw}^2 - r_d^2)}{r_{nw}^2} \tag{27}$$

For a partially depleted nanowire, the average electron concentration, averaged over the nanowire cross section, is given by

$$\bar{n}_{pd} = N_c e^{(\psi_0 - E_g/2)/kT} \left(\frac{r_d^2}{r_{nw}^2} + \frac{kT}{\chi} (1 - e^{\chi(r_d^2 - r_{nw}^2)/kTr_{nw}^2}) \right) \tag{28}$$

For a fully depleted nanowire, the average electron concentration is

$$\bar{n}_{fd} = N_c e^{(\psi_s - E_g/2)/kT} \frac{kT}{\chi} (e^{\chi/kT} - 1) \tag{29}$$

Equations 20−28 can now be combined to obtain the average electron density $\bar{n}$ of an n-type Si nanowire as a function of the donor density N_D for different nanowire diameters and interface trap level densities D_{it}. This is shown in Figure 21a for a D_{it} of 1×10^{12} eV^{-1} cm^{-2} and nanowire diameters ranging from 10 to 80 nm (the numbers beside the curves are the diameters in nanometers). For diameters ranging from 20 to 80 nm, one can observe a sharp decrease in the average electron concentration if the dopant density is smaller than a certain threshold value. This sharp decrease sets in when the nanowire changes from being partially depleted to being fully depleted; that is, when the diameter is equal to the critical diameter (see Figure 20b). Furthermore, Figure 21a reveals that, for example, a 14 nm nanowire would still be fully depleted—even at an extreme dopant concentration of 10^{20} cm^{-3}. At these small diameters, a proper surface passivation is essential.

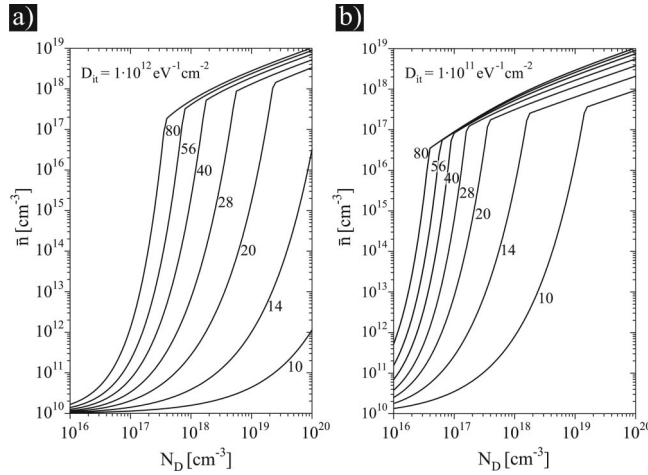


Figure 21. Average electron concentration $\bar{n}$ as a function of the donor concentration for various nanowire diameters and two different interface trap level densities D_{it}: (a) $D_{it} = 1 \times 10^{12}$ eV^{-1} cm^{-2}; (b) $D_{it} = 1 \times 10^{11}$ eV^{-1} cm^{-2}. The numbers near the curves indicate the nanowire diameter in nanometers. Dopant is P with a bulk ionization energy of 45 meV; temperature is 300 K.

In Figure 21b, a reduced D_{it} of 1×10^{11} eV^{-1} cm^{-2} is considered. One can see that the onset of full depletion is shifted to lower dopant densities. Due to the lower interface trap density, a 14 nm nanowire, which can be seen to be fully depleted in Figure 21a, is now fully depleted only for dopant concentrations smaller than about 2×10^{18} cm^{-3}. Comparing the average electron concentration of a 14 nm nanowire at a dopant concentration $N_D = 1 \times 10^{19}$ cm^{-3} in parts a and b of Figure 21 shows that, as a result of reducing the interface trap density by 1 order of magnitude, one would gain about 5 orders of magnitude in the effective charge carrier concentration. Such a characteristic has also been experimentally confirmed. Cui et al.[224] managed to decrease the resistance of silicon nanowires by a factor of 260 by a high temperature annealing of the nanowires.

It is also interesting to see in Figure 21b that at a nanowire diameter of 10 nm and a dopant concentration of 1×10^{20} cm^{-3} one would end up with an average electron concentration that is about 2 orders of magnitude smaller than the dopant concentration. This is clearly due to the reduced ionization efficiency.

The last major uncertainty for correlating resistivity with doping concentration is the charge carrier mobility. Charge carrier mobility depends on both dopant type and concentration. Hole mobilities are smaller than electron mobilities, and both decrease with dopant concentration as charge carriers scatter at the ionized dopant atoms.[193] Yet, impurity scattering is not the only relevant scattering mechanism; phonon scattering also plays an important role, in particular at low dopant densities. For Si nanowires, also the influence of the nanowire surface on the charge carrier mobility has to be taken into account. Considering thin Si nanowires having a high surface-to-volume ratio, one would expect a reduction of mobility because of increased surface scattering. This has been confirmed by simulations, which showed that surface scattering becomes crucial for nanowires of cross-sectional area smaller than 5 nm × 5 nm.[225] At these size ranges also, phonon scattering in nanowires differs from its bulk Si equivalent. According to Kotlyar et al.,[226] phonon scattering is increased due to an increased overlap between the electron and phonon wave function, which would cause a further mobility degradation.

Most experimental studies indeed indicate that charge carrier mobilities in silicon nanowires are somewhat smaller than those in bulk Si.[227−233] There are some studies, however, that report mobilities higher than those in bulk Si.[159,224] A possible explanation for the high mobility values obtained could be the crystallographic orientation of the nanowires. Cui et al.,[224] for example, measured mobilities in nanowires with 10−20 nm diameters,[224] synthesized by a method that according to an earlier report of the same group leads to a ⟨110⟩ orientation in this diameter range; and according to simulations of Buin et al.,[234] the hole mobility of ⟨110⟩ oriented silicon nanowires is significantly enhanced compared to that of bulk silicon.

Concerning a comparison of mobilities in Si nanowires to bulk Si values, one should be aware that the diameter dependence of the ionization efficiency may have a significant influence on measured mobilities. This is because dopant atoms that are not ionized do not, or at least not to the same extent, act as scattering centers for charge carriers. One should therefore not compare mobilities in silicon nanowires of a certain nominal doping concentration to bulk silicon values at the same nominal concentration, but rather to bulk silicon values at the same density of ionized dopants.

To summarize, interface traps at the Si/SiO_2 interface may significantly reduce the charge carrier concentration. The question whether mobilities in Si nanowires are comparable, greater, or smaller than mobilities in bulk Si does not seem to be fully decided yet. There is definitely a need for further investigations.

13. Summary and Open Questions

Much research work has already been done on chemical vapor deposition of silicon nanowires, on the synthesis of the nanowires itself, as well as on their properties. Nevertheless, a number of open questions still remain to be answered. The different Si nanowire growth methods were discussed in detail in section 2. From our point of view, chemical vapor deposition appears to be the method of choice when an in-place growth of epitaxial Si nanowires is envisaged. It offers versatility and controllability concerning morphology and electrical properties. However, some problems, especially concerning the control of growth orientation and kinking, as discussed in section 4, still need to be solved. Understanding the kinking process better could be essential for diminishing the percentage of kinked wires. Right now, the only way how to prevent nanowire kinking is to grow the nanowires within predefined templates; and it could be that templated growth is the only way how to realize 100% reliability regarding position and orientation. Solution-based synthesis techniques on the other hand seem to be the best method for the mass production of silicon nanowires, and the realization of solution based growth at atmospheric pressures is a major breakthrough. Regarding the choice of the catalyst material for VLS Si nanowire growth, we have seen in section 3 that there are several good options for growth at high temperatures. In particular, Pd and Ni seem attractive, as the position of their corresponding defect levels in Si is favorable. For low temperature CVD of Si nanowires, the three type-A catalysts, Au, Ag, and Al, appear to be the best choice. Al and Au give excellent growth results, but each comes with a major drawback: the sensitivity to oxidation being the one of Al and the creation of deep level defects being the one of Au. In view of the defect levels in Si, Ag would be far less harmful than Au, and it is somewhat astonishing that so little experimental results on the use of Ag as catalyst have been reported so far.

The synthesis of Si-based nanowire heterostructure, presented in section 5, is the logical extension of the work that has already been done on the growth of pure Si wires. The growth of both radial and axial heterostructures is attractive, as the electronic properties of the nanowire can strongly be modified by combining materials such as Si and Ge, for instance. Compared to planar heterostructures, axial heterostructure nanowires offer the decisive advantage that they can sustain much higher misfit-strain levels without causing dislocation formation. This theoretically predicted property of axial nanowire heterostructures still needs to be investigated in detail. The singular advantage of Ge-core−Si-shell nanowires is that the well-known problem with the Ge surface (there is no stable Ge oxide) could possibly be overcome by wrapping the Ge in Si. This is definitely a promising approach, also in view of potential investigations on the interplay between electronic properties and mechanical strain in nanowires. First, however, the problem associated with strain induced roughening of the shell needs to be solved satisfactorily.

The VLS mechanism has several interesting implications for the thermodynamics of the wire growth. The diameter expansion at the wire base is one of these implications. This expansion nicely reflects the nature of the surface-thermodynamical interaction between the liquid catalyst droplet and the growing wire. Concerning the simple model for the expansion, presented in section 7, one should, however, add that this model does not take the crystallography of Si into account. A deeper understanding of the influence of the crystallography on the wire shape in the initial phase of growth would be potentially valuable for controlling the nanowire growth direction. The surface tension criterion, discussed in section 8, also derives from the surface-thermodynamical interaction between droplet and nanowire. This criterion offers a potential explanation for the observation that Ga- or In-catalyzed VLS growth is more difficult than one would expect in the first place. The practical significance of the surface tension criterion is, however, unclear; mostly because it also still is undecided whether the problem with the type-B catalysts is caused by their insufficient Si solubility itself or rather by their too low surface tension. The probably best understood thermodynamic implication of the VLS growth mechanism concerns the diameter dependence of the growth velocity. As discussed in section 9, this diameter dependence is a direct consequence of the Gibbs−Thomson effect. Although the Gibbs−Thomson effect is a simple effect, its influence on the nanowire growth velocity shows some complexity. In particular, the question of the diameter dependence is related to the question whether it is more the Si incorporation into the droplet or the Si crystallization that determines the growth velocity. Detailed studies on the diameter and pressure dependence of the growth velocity could provide worthwhile information for a better understanding of the VLS mechanism.

The last part of this review was dedicated to the electrical properties of Si nanowires, starting with section 10 on vapor phase doping. It is obvious that a well-defined doping is a conditio sine qua non for Si nanowires with well-defined electrical properties. However, in contrast to what holds for bulk materials, the electrical properties of nanowires are not determined by the dopant concentration alone. There are several reasons for that. The first is that the dopant ionization

depends on the nanowire diameter, as explained in section 11. The second reason is that even if it were known to what extent the dopant atoms are ionized, the influence of the Si surface can often not be neglected. As shown in section 12, surface states at the Si surface can cause a considerable reduction of the charge carrier density. Depending on the quality of the surface passivation and the diameter of the nanowires, a certain minimum dopant density is required to obtain highly conductive nanowires. Otherwise, the nanowires simply behave as intrinsic silicon, despite being doped. The third reason why the correlation between dopant concentration and conductivity is more complex in Si nanowires is that the charge carrier mobility in Si nanowires could be different. Whether mobilities in Si nanowires indeed differ from bulk Si is a question of major concern, and a thorough and systematic study on mobilities in Si nanowires would be very valuable scientifically and technologically.

14. Acknowledgments

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15. References

(1) Treuting, R. G.; Arnold, S. M. *Acta Met.* **1957**, *5*, 598.
(2) Wagner, R. S.; Ellis, W. C. *Appl. Phys. Lett.* **1964**, *4*, 89.
(3) Schmidt, V.; Senz, S.; Gösele, U. *Z. Metallkd.* **2005**, *96*, 427.
(4) Schmidt, V.; Wittemann, J. V.; Senz, S.; Gösele, U. *Adv. Mater.* **2009**, *21*, 2681.
(5) Walch, S. P.; Dateo, C. E. *J. Phys. Chem. A* **2001**, *105*, 2015.
(6) Garnett, E. C.; Liang, W.; Yang, P. *Adv. Mater.* **2007**, *19*, 2946.
(7) Kayes, B. M.; Filler, M. A.; Putnam, M. C.; Kelzenberg, M. D.; Lewis, N. S.; Atwater, H. A. *Appl. Phys. Lett.* **2007**, *91*, 103110.
(8) Hochbaum, A. I.; Fan, R.; He, R.; Yang, P. *Nano Lett.* **2005**, *5*, 457.
(9) Lombardi, I.; Hochbaum, A. I.; Yang, P.; Carraro, C.; Maboudian, R. *Chem. Mater.* **2006**, *18*, 988.
(10) Givargizov, E. I. *J. Cryst. Growth* **1975**, *31*, 20.
(11) Nebol'sin, V. A.; Shchetinin, A. A.; Dolgachev, A. A.; Korneeva, V. V. *Inorg. Mater.* **2005**, *41*, 1256.
(12) Lew, K.-K.; Redwing, J. M. *J. Cryst. Growth* **2003**, *254*, 14.
(13) Chung, S. W.; Yu, J. Y.; Heath, J. R. *Appl. Phys. Lett.* **2000**, *76*, 2068.
(14) Wagner, R. S.; Ellis, W. C.; Jackson, K. A.; Arnold, S. M. *J. Appl. Phys.* **1964**, *35*, 2993.
(15) Greiner, E. S.; Gutowski, J. A.; Ellis, W. C. *J. Appl. Phys.* **1961**, *32*, 2489.
(16) Wagner, R. S.; Ellis, W. C. *Trans. Met. Soc. AIME* **1965**, *233*, 1053.
(17) Theuerer, H. C. *J. Electrochem. Soc.* **1961**, *108*, 649.
(18) Weyher, J. *Mater. Sci. Eng.* **1975**, *20*, 171.
(19) Ostwald, W. *Lehrbuch der Allgemeinen Chemie*; Engelmann: Leipzig, Germany, 1896; Vol. 2
(20) Lifshitz, I. M.; Slyozov, V. V. *J. Phys. Chem. Solids* **1961**, *19*, 35.
(21) Chakraverty, B. K. *J. Phys. Chem. Solids* **1967**, *28*, 2401.
(22) Wynblatt, P.; Gjostein, N. A. *Acta Met.* **1976**, *24*, 1165.
(23) Wynblatt, P. *Acta Met.* **1976**, *24*, 1175.
(24) Hannon, J. B.; Kodambaka, S.; Ross, F. M.; Tromp, R. M. *Nature* **2006**, *440*, 69.
(25) den Hertog, M. I.; Rouviere, J.-L.; Dhalluin, F.; Desre, P. J.; Gentile, P.; Ferret, P.; Oehler, F.; Baron, T. *Nano Lett.* **2008**, *8*, 1544.
(26) Wu, Y.; Cui, Y.; Huynh, L.; Barrelet, C. J.; Bell, D. C.; Lieber, C. M. *Nano Lett.* **2004**, *4*, 433.
(27) Schmidt, V.; Senz, S.; Gösele, U. *Nano Lett.* **2005**, *5*, 931.
(28) Givargizov, E. I. *J. Cryst. Growth* **1973**, *20*, 217.
(29) Schmid, H.; Björk, M. T.; Knoch, J.; Riel, H.; Riess, W. *J. Appl. Phys.* **2008**, *103*, 024304.
(30) Bootsma, G. A.; Gassen, H. J. *J. Cryst. Growth* **1971**, *10*, 223.
(31) Onischuk, A. A.; Strunin, V. P.; Ushakova, M. A.; Panfilov, V. N. *Int. J. Chem. Kinet.* **1998**, *30*, 99.
(32) Odden, J. O.; Egeberg, P. K.; Kjekshus, A. *Int. J. Chem. Kinet.* **2006**, *38*, 309.
(33) Ross, F. M.; Tersoff, J.; Reuter, M. C. *Phys. Rev. Lett.* **2005**, *95*, 146104.
(34) Kodambaka, S.; Hannon, J. B.; Tromp, R. M.; Ross, F. M. *Nano Lett.* **2006**, *6*, 1292.
(35) Hofmann, S.; Sharma, R.; Wirth, C. T.; Cervantes-Sodi, F.; Ducati, C.; Kasama, T.; Dunin-Borkowski, R. E.; Drucker, J.; Bennett, P.; Robertson, J. *Nat. Mater.* **2008**, *7*, 372.
(36) Kodambaka, S.; Tersoff, J.; Reuter, M. C.; Ross, F. M. *Phys. Rev. Lett.* **2006**, *96*, 096105.
(37) Sunkara, M. K.; Sharma, S.; Miranda, R.; Lian, G.; Dickey, E. C. *Appl. Phys. Lett.* **2001**, *79*, 1546.
(38) Hofmann, S.; Ducati, C.; Neill, R. J.; Piscanec, S.; Ferrari, A. C.; Geng, J.; Dunin-Borkowski, R. E.; Robertson, J. *J. Appl. Phys.* **2003**, *94*, 6005.
(39) Sharma, S.; Sunkara, M. K. *Nanotechnology* **2004**, *15*, 130.
(40) Iacopi, F.; Vereecken, P. M.; Schaekers, M.; Caymax, M.; Moelans, N.; Blanpain, B.; Richard, O.; Detavernier, C.; Griffiths, H. *Nanotechnology* **2007**, *18*, 505307.
(41) Westwater, J.; Gosain, D. P.; Usui, S. *Jpn. J. Appl. Phys.* **1997**, *36*, 6204.
(42) Wang, Y. F.; Lew, K. K.; Ho, T. T.; Pan, S. W.; Novak, L.; Dickey, E. C.; Redewing, T. S.; Mayer, J. M. *Nano Lett.* **2005**, *5*, 2139.
(43) Pan, L.; Lew, K. K.; Redwing, J. M.; Dickey, C. *J. Cryst. Growth* **2005**, *277*, 428.
(44) Kempa, T. J.; Tian, B.; Kim, D. R.; Hu, J.; Zheng, X.; Lieber, C. M. *Nano Lett.* **2008**, *8*, 3456.
(45) Wagner, R. S.; Doherty, C. J. *J. Electrochem. Soc.* **1968**, *115*, 93.
(46) Westwater, J.; Gosain, D. P.; Tomiya, S.; Usui, S.; Ruda, H. *J. Vac. Sci. Technol. B* **1997**, *15*, 554.
(47) Zhang, X.-Y.; Zhang, L.-D.; Meng, G.-W.; Li, G.-H.; Jin-Phillipp, N.-Y.; Phillipp, F. *Adv. Mater.* **2001**, *13*, 1238.
(48) Lew, K.-K.; Reuther, C.; Carim, A. H.; Redwing, J. M.; Martin, B. R. *J. Vac. Sci. Technol. B* **2002**, *20*, 389.
(49) Shimizu, T.; Xie, T.; Nishikawa, J.; Shingubara, S.; Senz, S.; Gösele, U. *Adv. Mater.* **2007**, *19*, 917.
(50) Holmes, J. D.; Johnston, K. P.; Doty, R. C.; Korgel, B. A. *Science* **2000**, *287*, 1471.
(51) Lu, X. M.; Hanrath, T.; Johnston, K. P.; Korgel, B. A. *Nano Lett.* **2003**, *3*, 93.
(52) Hanrath, T.; Korgel, B. A. *Adv. Mater.* **2003**, *15*, 437.
(53) Lee, D. C.; Hanrath, T.; Korgel, B. A. *Angew. Chem., Int. Ed.* **2005**, *44*, 3573.
(54) Tuan, H. Y.; Korgel, B. A. *Chem. Mater.* **2008**, *20*, 1239.
(55) Tuan, H.-Y.; Lee, D. C.; Korgel, B. A. *Angew. Chem.* **2006**, *45*, 5184.
(56) Tuan, H. Y.; Ghezelbash, A.; Korgel, B. A. *Chem. Mater.* **2008**, *20*, 2306.
(57) Heitsch, A. T.; Fanfair, D. D.; Tuan, H. Y.; Korgel, B. A. *J. Am. Chem. Soc.* **2008**, *130*, 5436.
(58) Schubert, L.; Werner, P.; Zakharov, N. D.; Gerth, G.; Kolb, F. M.; Long, L.; Gösele, U.; Tan, T. Y. *Appl. Phys. Lett.* **2004**, *84*, 4968.
(59) Zakharov, N. D.; Werner, P.; Gerth, G.; Schubert, L.; Sokolov, L.; Gösele, U. *J. Cryst. Growth* **2006**, *290*, 6.
(60) Zakharov, N.; Werner, P.; Sokolov, L.; Gösele, U. *Physica E* **2007**, *37*, 148.
(61) Fuhrmann, B.; Leipner, H. S.; Höche, H.-R.; Schubert, L.; Werner, P.; Gösele, U. *Nano Lett.* **2005**, *5*, 2524.
(62) Werner, P.; Zakharov, N. D.; Gerth, G.; Schubert, L.; Gösele, U. *Int. J. Mater. Res.* **2006**, *97*, 1008.
(63) Sivakov, S.; Andrä, G.; Gösele, U.; Christiansen, S. *Phys. Status Solidi A* **2006**, *203*, 3692.
(64) Sivakov, V.; Heyroth, F.; Falk, F.; Andrä, G.; Christiansen, S. *J. Cryst. Growth* **2007**, *300*, 288.
(65) Das Kanungo, P.; Zakharov, N.; Bauer, J.; Breitenstein, O.; Werner, P.; Goesele, U. *Appl. Phys. Lett.* **2008**, *92*, 263107.
(66) Morales, A. M.; Lieber, C. M. *Science* **1998**, *279*, 208.
(67) Zhang, Y. F.; Tang, Y. F.; Wang, N.; Lee, C. S.; Bello, I.; Lee, S. T. *Appl. Phys. Lett.* **1998**, *72*, 1835.
(68) Zhang, H. Z.; Yu, D. P.; Ding, Y.; Bai, Z. G.; Hang, Q. L.; Feng, S. Q. *Appl. Phys. Lett.* **1998**, *73*, 3396.
(69) Peng, H. Y.; Pan, Z. W.; Xu, L.; Fan, X. H.; Wang, N.; Lee, C.-S.; Lee, S.-T. *Adv. Mater.* **2001**, *13*, 317.
(70) Zhang, Y. F.; Tang, Y. H.; Peng, H. Y.; Wang, N.; Lee, C. S.; Bello, I.; Lees, S. T. *Appl. Phys. Lett.* **1999**, *75*, 1842.
(71) Zhou, G. W.; Zhang, Z.; Bai, Z. G.; Feng, S. Q.; Yu, D. P. *Appl. Phys. Lett.* **1998**, *73*, 677.
(72) Wang, N.; Tang, Y. H.; Zhang, Y. F.; Yu, D. P.; Lee, C. S.; Bello, I.; Lee, S. T. *Chem. Phys. Lett.* **1998**, *283*, 368.
(73) Yang, Y.-H.; Wu, S.-J.; Chiu, H. S.; Lin, P.-I.; Chen, Y.-T. 2004, *108*, 846.
(74) Wang, N.; Tang, Y. H.; Zhang, Y. F.; Lee, C. S.; Lee, S. T. *Phys. Rev. B* **1998**, *58*, 16024.
(75) Wang, N.; Zhang, Y. F.; Tang, Y. H.; Lee, C. S.; Lee, S. T. *Appl. Phys. Lett.* **1998**, *73*, 3902.
(76) Zhang, R.-Q.; Lifshitz, Y.; Lee, S.-T. *Adv. Mater.* **2003**, *15*, 635.
(77) Lee, S. T.; Zhang, Y. F.; Wang, N.; Tang, Y. H.; Bello, I.; Lee, C. S.; Chung, Y. W. *J. Mater. Res.* **1999**, *14*, 4503.
(78) Zhao, Y.; Yakobson, B. I. *Phys. Rev. Lett.* **2003**, *91*, 035501.

(79) Li, C.-P.; Lee, C.-S.; Ma, X.-L.; Wang, N.; Zhang, R.-Q.; Lee, S.-T. *Adv. Mater.* **2003**, *15*, 607.
(80) Tang, Y. H.; Sham, T. K.; Jürgensen, A.; Hu, Y. F.; Lee, C. S.; Lee, S. T. *Appl. Phys. Lett.* **2002**, *80*, 3709.
(81) Cui, Y.; Duan, X.; Hu, J.; Lieber, C. M. *J. Phys. Chem. B.* **2000**, *104*, 5213.
(82) Pan, Z. W.; Dai, Z. R. *J. Phys. Chem. B.* **2001**, *105*, 2507.
(83) Kolb, F. M.; Hofmeister, H.; Scholz, R.; Zacharias, M.; Gösele, U.; Ma, D. D.; Lee, S. T. *J. Electrochem. Soc.* **2004**, *151*, G472.
(84) Kolb, F. M.; Hofmeister, H.; Zacharias, M.; Gösele, U. *Appl. Phys. A: Mater. Sci. Process.* **2005**, *80*, 1405.
(85) Shi, W. S.; Peng, H. Y.; Zheng, Y. F.; Wang, N.; Shang, N. G.; Pan, Z. W.; Lee, C. S.; Lee, S. T. *Adv. Mater.* **2000**, *12*, 1343.
(86) Gole, J. L.; Stout, J. D.; Rauch, W. L.; Wang, Z. L. *Appl. Phys. Lett.* **2000**, *76*, 2346.
(87) Zhang, Z.; Fan, X. H.; Xu, L.; Lee, C. S.; Lee, S. T. *Chem. Phys. Lett.* **2001**, *337*, 18.
(88) http://www.british biocell.co.uk/.
(89) Shchetinin, A. A.; Nebol'sin, V. A.; Kozenkov, O. D.; Tatarenkov, A. F.; Dunaev, A. I. N. E. P. *Inorg. Mater.* **1991**, *27*, 1137.
(90) Allen, J. E.; Hemesath, E. R.; Perea, D. E.; Lensch-Falk, J. L.; Li, Z. Y.; Yin, F.; Gass, M. H.; Wang, P.; Bleloch, A. L.; Palmer, R. E.; Lauhon, L. J. *Nat. Nanotechnol.* **2008**, *3*, 168.
(91) Perea, D. E.; Allen, J. E.; May, S. J.; Wessels, B. W.; Seidman, D. N.; Lauhon, L. J. *Nano Lett.* **2006**, *6*, 181.
(92) Tatsumi, Y.; Shigi, M.; Hirata, M. *J. Phys. Soc. Jpn.* **1978**, *45*, 703.
(93) Nebol'sin, V. A.; Shchetinin, A. A. *Inorg. Mater.* **2003**, *39*, 899.
(94) Osada, Y.; Nakayama, H.; Shindo, M.; Odaka, T.; Ogata, Y. *J. Electrochem. Soc.* **1979**, *126*, 31.
(95) Wang, Y.; Schmidt, V.; Senz, S.; Gösele, U. *Nat. Nanotechnol.* **2006**, *1*, 186.
(96) Whang, S. J.; Lee, S. J.; Yang, W.; Cho, B. J.; Liew, Y. F.; Li, K.; Bera, L. K.; Tung, C. H.; Kwong, D. L. Conference Abstract 210th ECS Meeting; 2006; abstract 0097.
(97) Whang, S. J.; Lee, S. J.; Yang, W. F.; Cho, B. J.; Liew, Y. F.; Kwong, D. L. *Electrochem. Solid-State Lett.* **2007**, *10*, E11.
(98) Whang, S. J.; Lee, S. J.; Chi, D. Z.; Yang, W. F.; Cho, B. J.; Liew, Y. F.; Kwong, D. L. *Nanotechnology* **2007**, *18*, 275302.
(99) Bae, J.; Kulkarni, N. N.; Zhou, J. P.; Ekerdt, J. G.; Shih, C. K. *J. Cryst. Growth* **2008**, *310*, 4407.
(100) Miyamoto, Y.; Hirata, M. *Jpn. J. Appl. Phys.* **1976**, *15*, 1159.
(101) Yao, Y.; Fan, S. *Mater. Lett.* **2007**, *61*, 177.
(102) Arbiol, J.; Kalache, B.; Roca i Cabarrocas, P.; Morante, J. R.; Fontcuberta i Morral, A. *Nanotechnology* **2007**, *18*, 305606.
(103) Gu, Q.; Dang, H.; Cao, J.; Zhao, J.; Fan, S. *Appl. Phys. Lett.* **2000**, *76*, 3020.
(104) Feng, S. Q.; Yu, D. P.; Zhang, H. Z.; Bai, Z. G.; Ding, Y. *J. Cryst. Growth* **2000**, *209*, 513.
(105) Liu, Z. Q.; Xie, S. S.; Zhou, W. Y.; Sun, L. F.; Li, Y. B.; Tang, D. S.; Zou, X. P.; Wang, C. Y.; Wang, G. *J. Cryst. Growth* **2001**, *224*, 230.
(106) Barsotti, R. J.; Fischer, J. E.; Lee, C. H.; Mahmood, J.; Adu, C. K. W.; Eklund, P. C. *Appl. Phys. Lett.* **2002**, *81*, 2866.
(107) Givargizov, E. I.; Sheftal, N. N. *J. Cryst. Growth* **1971**, *9*, 326.
(108) Iacopi, F.; Richard, O.; Eichhammer, Y.; Bender, H.; Vereecken, P. M.; de Gendt, S.; Heyns, M. *Electrochem. Solid-State Lett.* **2008**, *11*, K98.
(109) James, D. W. F.; Lewis, C. *Br. J. Appl. Phys.* **1965**, *16*, 1089.
(110) Jin, S.; Li, Q.; Lee, C. S. *Phys. Status Solidi A* **2001**, *188*, R1.
(111) Tatsumi, Y.; Hirata, M.; Yamada, K. *J. Phys. Soc. Jpn.* **1981**, *50*, 2288.
(112) Weyher, J. *J. Cryst. Growth* **1978**, *43*, 235.
(113) Baron, T.; Gordon, M.; Dhalluin, F.; Ternon, C.; Ferret, P.; Gentile, P. *Appl. Phys. Lett.* **2006**, *89*, 233111.
(114) Jeon, M.; Kamisako, K. *Mater. Lett.* **2009**, *63*, 777.
(115) Kamins, T. I.; Williams, R. S.; Chen, Y.; Chang, Y.-L.; Chang, Y. A. *Appl. Phys. Lett.* **2000**, *76*, 562.
(116) Kamins, T. I.; Williams, R. S.; Basile, D. P.; Hesjedal, T.; Harris, J. S. *J. Appl. Phys.* **2001**, *89*, 1008.
(117) Sharma, S.; Kamins, T. I.; Williams, R. S. *J. Cryst. Growth* **2004**, *267*, 613.
(118) Yu, J. Y.; Chung, S. W.; Heath, J. R. *J. Phys. Chem. B* **2000**, *104*, 11864.
(119) Wakaser, B. A.; Reuter, M. C.; Khayyat, M. M.; Wen, C.-Y.; Haight, R.; Guha, S.; Ross, F. M. *Nano Lett.* **2009**, *9*, 3296.
(120) Majni, G.; Ottaviani, G. *Appl. Phys. Lett.* **1977**, *31*, 125.
(121) Weber, L. *Metall. Mater. Trans. A* **2002**, *33A*, 1145.
(122) Geiger, F.; Busse, C. A.; Loehrke, R. I. *Int. J. Thermophys.* **1987**, *8*, 425.
(123) Massalski, T. B.; Okamoto, H.; Subramanian, P.; Kacprzak, L. *Binary Alloy Phase Diagrams*, 2nd ed.; ASM International: Materials Park, OH, 1990; Vol. 1-3
(124) Ge, S.; Jiang, K.; Lu, X.; Chen, Y.; Wang, R.; Fan, S. *Adv. Mater.* **2005**, *17*, 56.
(125) Wagner, R. S. *J. Appl. Phys.* **1967**, *38*, 1554.
(126) Ma, D. D. D.; Lee, C. S.; Au, F. C. K.; Tong, S. Y.; Lee, S. T. *Science* **2003**, *299*, 1874.
(127) Carmi, A. H.; Lew, K.-K.; Redwing, J. M. *Adv. Mater.* **2001**, *13*, 1489.
(128) Fontcuberta i Morral, A.; Arbiol, J.; Prades, J. D.; Cirera, A.; Morante, J. R. *Adv. Mater.* **2007**, *19*, 1347.
(129) Kailer, A.; Gogotsi, Y. G.; Nickel, K. G. *J. Appl. Phys.* **1997**, *81*, 3057.
(130) Meade, R. D.; Vanderbilt, D. *Phys. Rev. Lett.* **1989**, *63*, 1404.
(131) Twesten, R. D.; Gibson, J. M. *Phys. Rev. B* **1994**, *50*, 17628.
(132) van Heys, J.; Pehlke, E. *Phys. Rev. B* **2005**, *72*, 125351.
(133) Kohno, H.; Ozaki, N.; Yoshida, H.; Tanaka, K.; Takeda, S. *Cryst. Res. Technol.* **2003**, *38*, 1082.
(134) Chen, Y.-W.; Tang, Y.-H.; Pei, L.-Z.; Guo, C. *Adv. Mater.* **2005**, *17*, 564.
(135) De Crescenzi, M.; Castruzzi, P.; Scarselli, M.; Diociaiuti, M.; Chaudharis, P. s.; Balasubramanian, C.; Bhave, T. M.; Bhoraskar, S. V. *Appl. Phys. Lett.* **2005**, *86*, 231901.
(136) Perepichka, D. F.; Rosei, F. *Small* **2006**, *2*, 22.
(137) Tang, Y. H.; Pei, L. Z.; Chen, Y. W.; Guo, C. *Phys. Rev. Lett.* **2005**, *95*, 116102.
(138) Yamada, S.; Fujiki, H. *Jpn. J. Appl. Phys.* **2006**, *45*, L837.
(139) Tersoff, J.; LeGoues, F. K. *Phys. Rev. Lett.* **1994**, *72*, 3570.
(140) Ertekin, E.; Greaney, P. A.; Sands, T. D.; Chrzan, D. C. Mater. Res. Soc. Symp. Proc. 2003, *737*, F10.4.1
(141) Kästner, G.; Gösele, U. *Philos. Mag.* **2004**, *84*, 3803.
(142) Björk, M. T.; Ohlsson, B. J.; Sass, T.; Persson, A. I.; Thelander, C.; Magnusson, M. H.; Deppert, K.; Wallenberg, L. R.; Samuelson, L. *Nano Lett.* **2002**, *2*, 87.
(143) Kasper, E. *Phys. Scr.* **1991**, *T35*, 232.
(144) Wu, Y.; Fan, R.; Yang, P. *Nano Lett.* **2002**, *2*, 83.
(145) Redwing, J. M.; Lew, K.-K.; Bogart, T. E.; Pan, L.; Dickey, E. C.; Carim, A. H.; Wang, Y.; Cabassi, M. A.; Mayer, T. S. *Proc. SPIE—Int. Soc. Opt. Eng.* **2004**, *5361*, 52.
(146) Hanke, M.; Eisenschmidt, C.; Werner, P.; Zakharov, N. D.; Syrowatka, F.; Heyroth, F.; Schäfer, P.; Konovalov, O. *Phys. Rev. B* **2007**, *75*, 161303.
(147) Dujardin, R.; Poydenot, V.; Devillers, T.; Favre-Nicolin, V.; Gentile, P.; Barski, A. *Appl. Phys. Lett.* **2006**, *89*, 153129.
(148) Clark, T. E.; Nimmatoori, P.; Lew, K.-K.; Pan, L.; Redwing, J. M.; Dickey, E. C. *Nano Lett.* **2008**, *8*, 1246.
(149) Lu, W.; Xiang, J.; Timko, B. P.; Wu, Y.; Lieber, C. M. *Proc. Natl. Acad. Sci.* **2005**, *102*, 10046.
(150) Goldthorpe, I. A.; Marshall, A. F.; McIntyre, P. C. *Nano Lett.* **2008**, *8*, 4081.
(151) Colin, J.; Grilhé, J.; Junqua, N. *Philos. Mag. A* **1997**, *76*, 793.
(152) Gao, H.; Nix, W. D. *Annu. Rev. Mater. Sci.* **1999**, *29*, 173.
(153) Liang, Y.; Nix, W. D.; Griffin, P. B.; Plummer, J. D. *J. Appl. Phys.* **2005**, *97*, 043519.
(154) Yang, F.; Song, W. *Int. J. Solids Struct.* **2006**, *43*, 6767.
(155) Wang, H.; Upmanyu, M.; Ciobanu, C. V. *Nano Lett.* **2008**, *8*, 4305.
(156) Schmidt, V.; McIntyre, P. C.; Gösele, U. *Phys. Rev. B* **2008**, *77*, 235302.
(157) Lauhon, L. J.; Gudiksen, M. S.; Wang, D.; Lieber, C. M. *Nature* **2002**, *420*, 57.
(158) Xiang, J.; Lu, W.; Hu, Y.; Wu, Y.; Yan, H.; Lieber, C. M. *Nature* **2006**, *441*, 489.
(159) Wu, Y.; Xiang, J.; Yang, C.; Lu, W.; Lieber, C. M. *Nature* **2004**, *430*, 61.
(160) Maex, K.; van Rossum, M. *Properties of metal silicides*; INSPEC: London, 1995.
(161) Lin, Y.-C.; Lu, K.-C.; Wu, W.-W.; Bai, J.; Chen, L. J.; Tu, K. N.; Huang, Y. *Nano Lett.* **2008**, *8*, 913.
(162) Weber, W. M.; Geelhaar, L.; Graham, A. P.; Unger, E.; Duesburg, G. S.; Liebau, M.; Pamler, W.; Cheze, C.; Riechert, H.; Lugli, P.; Kreupl, F. *Nano Lett.* **2006**, *6*, 2660.
(163) Gibbs, J. W. In *The Scientific Papers of J. Williard Gibbs, PH.D., LL.D.*; Longmans, Green, and Co.: London, New York, Bombay, 1906; Vol. I. Thermodynamics; Chapter 3, pp 315—318.
(164) Shuttleworth, R. *Proc. Phys. Soc. A* **1950**, *63*, 444.
(165) Cahn, J. W. *Acta Met.* **1980**, *28*, 1333.
(166) Tanaka, T.; Hara, S. *Z. Metallkd.* **2001**, *92*, 467.
(167) Dinsdale, A. T. *Calphad* **1991**, *15*, 317.
(168) Chevalier, P.-Y. *Thermochim. Acta* **1988**, *130*, 33.
(169) Jacobs, M. H. G.; Spencer, P. J. 1996, *20*, 307.
(170) *CRC Handbook of chemistry and physics*, 80th ed.; CRC Press: Boca Raton, London, New York, Washington, DC, 1999; Chapter 4, pp 37—194.
(171) Wittenberg, L. J.; DeWitt, R. *J. Chem. Phys.* **1972**, *56*, 4526.
(172) Keene, B. J. *Int. Mater. Rev.* **1993**, *38*, 157.

(173) Tyson, W. R.; Miller, W. A. *Surf. Sci.* **1977**, *62*, 267.
(174) Gibbs, J. W. In *The Scientific Papers of J. Williard Gibbs, PH.D., LL.D.*; Dover Publications: New York, 1961; Vol. I. Thermodynamics; Chapter 3, pp 287−288.
(175) Rowlinson, J. S.; Widom, B. In *Molecular Theory of Capillarity*; Dover Publications: Mineola, NY, 2002; Chapter 8, p 209.
(176) Shchetinin, A. A.; Darinskii, B. M.; Kozenkov, O. D.; Nebol'sin, V. A. *Inorg. Mater.* **1990**, *26*, 1157.
(177) Wakayama, Y.; Tanaka, S. *Surf. Sci.* **1999**, *420*, 190.
(178) Givargizov, E. I. *Highly Anisotropic Crystals*; Reidel: Dordrecht, 1987.
(179) Ressel, B.; Prince, K. C.; Heun, S.; Homma, Y. *J. Appl. Phys.* **2003**, *93*, 3886.
(180) Satunkin, G. A.; Tatarchenko, V. A. *Kristallografiya* **1985**, *30*, 772.
(181) Tatarchenko, Y. A. In *Shaped Crystal Growth*; Kluwer Academic: Dordrecht, 1993; Chapter 1, pp 197−206.
(182) Schmidt, V.; Senz, S.; Gösele, U. *Appl. Phys. A: Mater. Sci. Process.* **2005**, *80*, 445.
(183) Rowlinson, J. S.; B., W. *Molecular Theory of Capillarity*; Dover Publications: Mineola, NY, 2002.
(184) Chen, P.; Gaydos, J.; Neumann, A. W. *Langmuir* **1996**, *12*, 5956.
(185) Naidich, Y. V.; Perevertailo, V. M.; Obushchak, L. P. *Zh. Fiz. Khim.* **1975**, *49*, 1554.
(186) Jaccodine, R. J. *J. Electrochem. Soc.* **1963**, *110*, 524.
(187) Kikkawa, J.; Ohno, Y.; Takeda, S. *Appl. Phys. Lett.* **2005**, *86*, 123109.
(188) Schmid, H.; Björk, M. T.; Knoch, J.; Karg, S.; Riel, H.; Riess, W. *Nano Lett.* **2009**, *9*, 173.
(189) Schmidt, V.; Senz, S.; Gösele, U. *Phys. Rev. B* **2007**, *75*, 045335.
(190) Tan, T. Y.; Li, N.; Gösele, U. *Appl. Phys. Lett.* **2003**, *83*, 1199.
(191) Tan, T. Y.; Li, N.; Gösele, U. *Appl. Phys. A: Mater. Sci. Process.* **2004**, *78*, 519.
(192) Dhalliun, F.; Desré, P. J.; den Hertog, M. I.; Rouviere, J.; Ferret, P.; Gentile, P.; Baron, T. *J. Appl. Phys.* **2007**, *102*, 094906.
(193) Sze, S. M. *Physics of Semiconductor Devices*, 2nd ed.; Wiley: New York, 1981.
(194) Fahey, P. M.; Griffin, P. B.; Plummer, J. D. *Rev. Mod. Phys.* **1989**, *61*, 289.
(195) Peelaers, H.; Partoens, B.; Peeters, F. M. *Nano Lett.* **2006**, *6*, 2781.
(196) Schmidt, V.; Riel, H.; Senz, S.; Karg, S.; Riess, W.; Gösele, U. *Small* **2006**, *2*, 85.
(197) Fukata, N.; Chen, J.; Sekiguchi, T.; Okada, N.; Murakami, K.; Tsurui, T.; Ito, S. *Appl. Phys. Lett.* **2006**, *89*, 203109.
(198) Fukata, N.; Chen, J.; Sekiguchi, T.; Matsushita, S.; Oshima, T.; Uchida, N.; Murakami, K.; Tsurui, T.; Ito, S. *Appl. Phys. Lett.* **2007**, *90*, 153117.
(199) Gudiksen, M. S.; Lauhon, L. J.; Wang, J.; Smith, D. C.; Lieber, C. M. *Nature* **2002**, *415*, 617.
(200) Yang, C.; Zhong, Z.; Lieber, C. M. *Science* **2005**, *310*, 1304.
(201) Lew, K.-K.; Pan, L.; Bogart, T. E.; Dilts, S. M.; Dickey, E. C.; Redwing, J. M.; Wang, Y. F.; Cabassi, M.; Mayer, T. S.; Novak, S. W. *Appl. Phys. Lett.* **2004**, *85*, 3101.
(202) White, R. T.; Espino-Rios, R. L.; Rodgers, D. S.; Ring, M. A.; O'Neal, H. E. *Int. J. Chem. Kinet.* **1985**, *17*, 1029.
(203) Jasinski, J. M.; Gates, S. M. *Acc. Chem. Res.* **1991**, *24*, 9.
(204) Diarra, M.; Niquet, Y. M.; Delerue, C.; Allan, G. *Phys. Rev. B* **2007**, *75*, 045301.
(205) Niquet, Y. M.; Lherbier, A.; Quang, N. H.; Fernández-Serre, M. V.; Blase, X.; Delerue, C. *Phys. Rev. B* **2006**, *73*, 165319.
(206) Diarra, M.; Delerue, C.; Niquet, Y. M.; Allan, G. *J. Appl. Phys.* **2008**, *103*, 073703.
(207) Björk, M. T.; Schmid, H.; Knoch, J.; Riel, H.; Riess, W. *Nat. Nanotechnol.* **2009**, *4*, 103.
(208) Deal, B. E. *IEEE Trans. Electron Devices* **1980**, *ED-27*, 606.
(209) White, M. H.; Cricchi, J. R. *IEEE Trans. Electron Devices* **1972**, *ED-19*, 1280.
(210) Nishi, Y. *Jpn. J. Appl. Phys.* **1966**, *5*, 333.
(211) Nishi, Y. *Jpn. J. Appl. Phys.* **1971**, *10*, 52.
(212) Nishi, Y.; Ohwada, A.; Tanaka, K. *Jpn. J. Appl. Phys.* **1972**, *11*, 85.
(213) Griscom, D. L. *Phys. Rev. B* **1980**, *22*, 4192.
(214) Caplan, P. J.; Poindexter, E. H.; Deal, B. E.; Razouk, R. R. *J. Appl. Phys.* **1979**, *50*, 5847.
(215) Lenahan, P. M.; Dressendorfer, P. V. *Appl. Phys. Lett.* **1982**, *41*, 542.
(216) Lenahan, P. M.; Dressendorfer, P. V. *J. Appl. Phys.* **1983**, *54*, 1457.
(217) Lenahan, P. M.; Dressendorfer, P. V. *Appl. Phys. Lett.* **1984**, *44*, 96.
(218) Kim, Y. Y.; Lenahan, P. M. *J. Appl. Phys.* **1988**, *64*, 3551.
(219) Johnson, N. M.; Biegelsen, D. K.; Moyer, M. D.; Chang, S. T.; Poindexter, E. H.; Caplan, P. J. *Appl. Phys. Lett.* **1983**, *43*, 563.
(220) Poindexter, E. H.; Caplan, P. J.; Deal, B. E.; Razouk, R. R. *J. Appl. Phys.* **1981**, *52*, 879.
(221) Schmidt, V.; Senz, S.; Gösele, U. *Appl. Phys. A: Mater. Sci. Process.* **2007**, *86*, 187.
(222) Seo, K. I.; Sharma, S.; Yasseri, A. A.; Stewart, D. R.; Kamins, T. I. *Electrochem. Solid-State Lett.* **2006**, *9*, G69.
(223) Kimukin, I.; Islam, M. S.; Williams, R. S. *Nanotechnology* **2006**, *17*, S240.
(224) Cui, Y.; Zhong, Z.; Wang, D.; Wang, W. U.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 149.
(225) Ramayya, E. B.; Vasileska, D.; Goodnick, S. M.; Knezevic, I. *J. Appl. Phys.* **2008**, *104*, 063711.
(226) Kotlyar, R.; Obradovic, B.; Matagne, P.; Stettler, M.; Giles, M. D. *Appl. Phys. Lett.* **2004**, *84*, 5270.
(227) Wang, D.; Sheriff, B. A.; Heath, J. R. *Nano Lett.* **2006**, *6*, 1096.
(228) Gunawan, O.; Sekaric, L.; Majumdar, A.; Rooks, M.; Appenzeller, J.; Sleight, J. W.; Guha, S.; Haensch, W. *Nano Lett.* **2008**, *8*, 1566.
(229) Ho, T.-T.; Wang, Y.; Eichfeld, S.; Lew, K.-K.; Liu, B.; Mohney, S. E.; Redwing, J. M.; Mayer, T. S. *Nano Lett.* **2008**, *8*, 4359.
(230) Zheng, G.; Lu, W.; Jin, S.; Lieber, C. M. *Adv. Mater.* **2004**, *16*, 1890.
(231) Duan, X.; Niu, C.; Sahi, V.; Chen, J.; Parce, J. W.; Empedocles, S.; Goldman, J. L. *Nature* **2003**, *425*, 274.
(232) Björk, M. T.; Hayden, O.; Schmid, H.; Riel, H.; Riess, W. *Appl. Phys. Lett.* **2007**, *90*, 142110.
(233) Goldberger, J.; Hochbaum, A. I.; Fan, R.; Yang, P. *Nano Lett.* **2006**, *6*, 973.
(234) Buin, A. K.; Verma, A.; Svizhenko, A.; Anantram, M. P. *Nano Lett.* **2008**, *8*, 760.
(235) Tang, Y. H.; Zhang, Y. F.; Wang, N.; Lee, C. S.; Han, X. D.; Bello, I.; Lee, S. T. *J. Appl. Phys.* **1999**, *85*, 7981.
(236) Björk, M. T.; Knoch, J.; Schmid, H.; Riel, H.; Riess, W. *Appl. Phys. Lett.* **2008**, *92*, 193504.

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